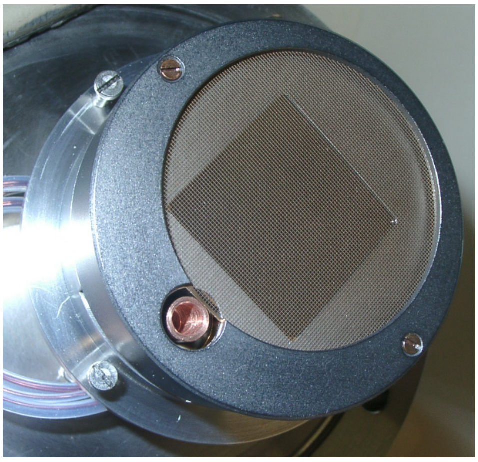
Manual

Delayline Detector DLD-3030



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1 Table of Content

2 Introduction

2.1 General Information

This manual is intended to assist users in the installation, operation and maintenance of the Delayline Detector DLD 3030 with integrated mini lenses. It is divided into 12 chapters. The chapter “Introduction” contains a brief description of the DLD. The chapter “Installation” refers to installation and cabling. One chapter describes the USB driver installation. Chapter “Principle of Operation” explains the theory of operation of the DLD. 3 chapters describe the technical details of the DLD 3030 readout package and chapter “Operation of the DLD” describes the operation of the DLD. The final chapters contain amongst others technical details about the microchannel plates and the delayline detector.

2.2 Safety Instructions

Caution!

Please read this manual carefully, before performing any electrical or electronic operations and strictly follow the safety rules given within this manual.

2.3 General Overview of the System

The Surface Concept delayline detectors are particularly developed for the needs of 1D(x), 2D(x,t), 2D(x,y) or 3D(x,y,t) area and time detection of electrons, ions, x-ray and UV-light.

The DLD 3030 consists of a Chevron microchannel plate stack and two layers (x, y) of meander structured delaylines. The image is sampled by the DLD readout electronics with a typ. image size of 400 pixels x 400 pixels

The 3D (x, y, t) detection bases on the measurement of time differences and time sums of signals, with a high temporal resolution in one device. The count rate can reach up to 2.0 MHz in the commonly used 4-fold coincidence measurement.

Typical applications are:

- imaging of parallel incident particle beams, particularly electrons
- spatially resolved time of flight spectroscopy in 2D/time resolved mode
- time referenced imaging of electrons excited by repetitive driven sources

and in energy analyzers:

- Fermi surface mapping, band mapping, photoelectron diffraction measurements, and similar angular dispersion experiments in 2D mode
- XPS, UPS, ESCA and AES in virtual channel mode
- Stroboscopic experiments in 2D/time resolved mode

3 Installation

3.1 Initial Inspection

Visual inspection of the system is required to ensure that no damage has occurred during shipping. Should there be any signs of damage, please contact SURFACE CONCEPT immediately. Please check the delivery according to the packing list (see Table 1) for completeness.

1. High Resolution USB 2.0–TDC including power cable
2. USB 2.0 cable
3. Pulse processing unit ACU 3.4.2
4. 1x DLD readout cable (HDMI)
5. 5x copper screws for mounting detector head (one spare screw)
6. Delayline detector unit (delivered in a vacuum container)

Table 1: Packing list for the Delayline Detector

3.2 Installation

3.2.1 Mounting the delayline detector

Release the M8 screws of the transport container and carefully pull out the detector. The container has been filled with argon gas.
Remove the two M3 screws (see Figure 1), to dismount the detector head from the CF100 base. To do so, first open the M3 nuts and then unscrew the M3 screws.

There are two sets of cabling connecting the detector head with the base flange. The HV cabling and the signal cabling. The HV cables end in 6 pin plug on the back side of the detector head. This plug can be unplugged for easier mounting of the detector. The signal cables are connected directly to the 4-fold SMB feed-through. If a mounting of the detector is not possible without dismounting the signal cables, then the 4-fold SMB feed-through must be opened and the cables must be disconnected, by carefully pulling off the single plugs (see section 6 for further details).

Caution!

The inner core of the signal cables is very sensitive to bending, especially on the contact point to the plug. Be very careful when disconnecting the plugs from the SMB feed-throughs, as the plugs break off very easily. A hint: try to prevent a relative movement of the plug connected to the inner core of a signal cable to the plug connected to the corresponding cable shield. Best would be to always fasten both plugs and to pull them off (or plug them on) simultaneously.

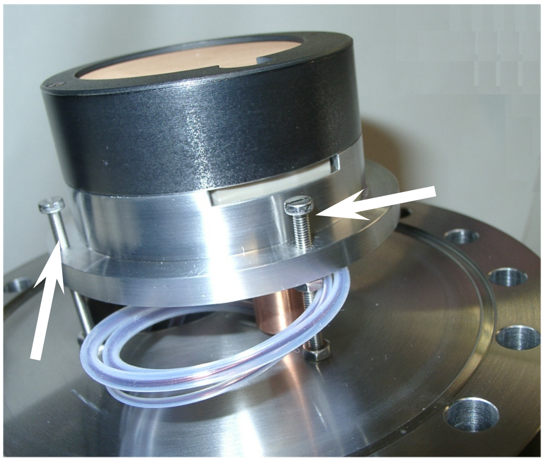


Figure 1: Dismounting the detector head.

There are 5 M3 copper screws included in the delivery, which can be used to mount the detector in the analyzer (see Figure 2).

Figure 2: Copper screws for detector mounting

Caution!

The microchannel plates in front of the detector should be protected from exposure to particle contamination. Particles that stick to the plate can be removed by using a single-hair brush carefully and/or dry nitrogen. Reading of the instructions "microchannel plates" in chapter 10 is strongly recommended.

3.2.2 Cabling and High Voltage

The general connection scheme of the delayline detector including its readout package is shown in Figure 3.

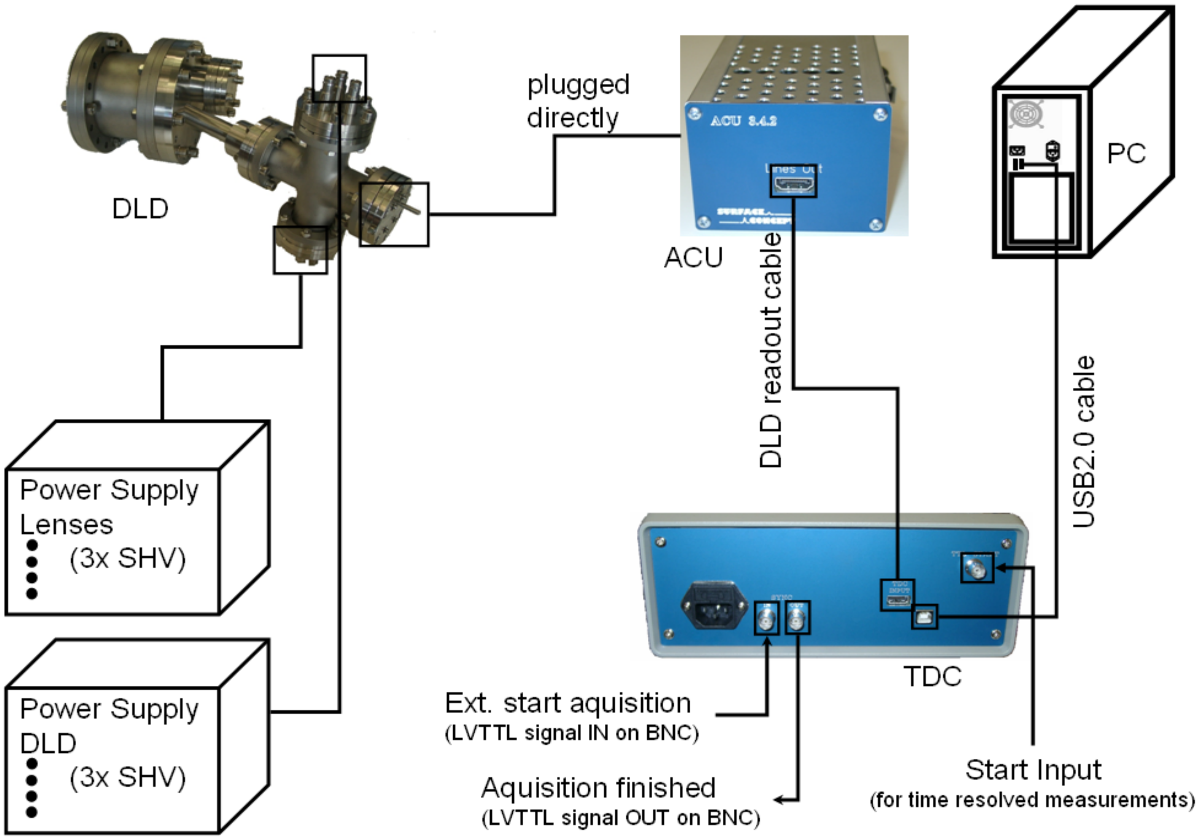


Figure 3: Connection scheme of the delayline detector and readout package

The pulse processing unit ACU 3.4.2 can be connected directly to the DLD 4-fold SMB feed-trough. The hole in the front plate is the counterpart to the metal pin on the feed-through. Two clips are mounded to the housing of the ACU 3.4.2. Attach them to the fastening bolds on the feed-through to fix the ACU 3.4.2.

Connect one end of the DLD readout cable to the "Lines Out" socket on the front of the ACU 3.4.2. The other end needs to be connected to the "TDC Input" socket at the rear panel of the USB2.0-TDC. To perform time measurements in respect to an external clock, provide start pulses to the start input of the TDC. Use the BNC socket named "TTL Start" to apply standard TTL signals.

Use the USB 2.0 cable to connect the USB2.0-TDC to the PC and follow the instructions for installing the device driver if connected for the first time. If the device driver is already installed, the USB connection is established automatically. Do not use PC front panel USB connectors; they are often restricted in performance. For further details in driver installation see chapter 4.

There are two CF40 flanges with 3 SHV feed-throughs each (in total 6) for high voltage supply. One flange is for the delayline detector and the second one for the mini lenses.
The SHV flange for the delayline detector holds the connection for the MCP front (F), the MCP Back (B) and the detector anode (H). The corresponding labeling F, B and H can be found on the feed-throughs.
The SHV flange for the mini lenses holds the connection for the front lens (LV), the middle lens (LM) and the back lens (LH). The corresponding labeling LV, LM and LH can be found again on the feed-throughs.

Note: Be sure that all voltages are settled to zero before connecting the high voltage cables to the detector.

Connect the power cable to the main connector and plug the USB cable into the PC. Switch on the TDC and follow the instructions for installing the device driver if connected for the first time. If the device driver is already installed, the USB connection is established automatically.

Caution!

Finish the complete cabling before the TDC is turned on and the GUI monitor software is started. Also, close the software and turn off the TDC before performing any changes of the cabling. This applies especially to the connection and disconnection of the start input of the TDC. The start input of the TDC cannot handle pulses which are arriving in a time interval of smaller than 150 ns, as they are produced by e.g. connecting to and disconnecting from the start input respectively.

Caution!

Don't start the detector operation before you are familiar with the detailed descriptions of chapter 9 within this manual.

3.2.3 Recommended system requirements

Read-out of the USB2.0–TDC is done with a standard PC via USB2.0. For the PC the following system requirements are highly recommended:

- Processor: 1.6 Ghz
- RAM: 1GB
- Windows XP / Windows 2000
- USB 2.0 (no front panel connector)
- Monitor resolution: in Y min. 864 pixel (most critical), in X min. 1024 pixel

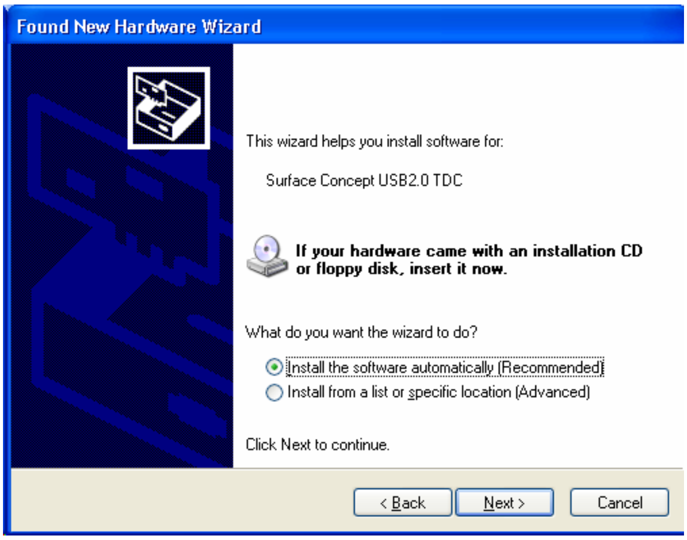
Note: The use of USB2.0 for the readout of the TDC is highly recommended. In principle the readout of the TDC is compatible to USB1.0, but the required data transfer rates are not reached. Do not use PC front panel USB connectors; they are often restricted in performance.

4 USB 2.0 driver Installation

- First, log on as Administrator. Close all applications on your PC. If you are using any anti-virus or firewall software, close them (or disable them). Connect the USB cable to your Windows System with USB2.0 enabled. Windows will find a new hardware, and the "Found New Hardware Wizard" will launch. To continue, select "No, not this time" (not looking for windows updates) and "click "Next>".

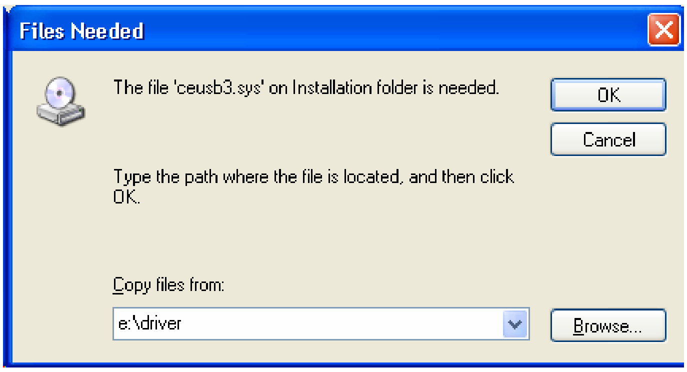
- Insert the CD-ROM, included in the delivery, into the PC's CD-ROM drive.

- Select "Install the software automatically (Recommended)" and Click "Next>".

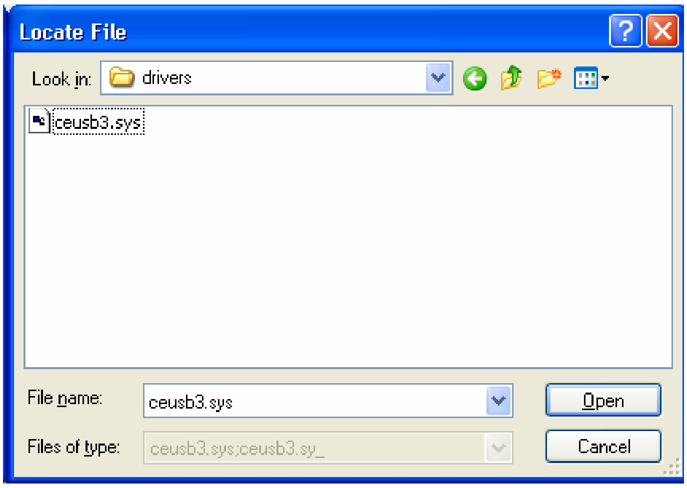


- Continue Installation although the Windows XP capability test failed.

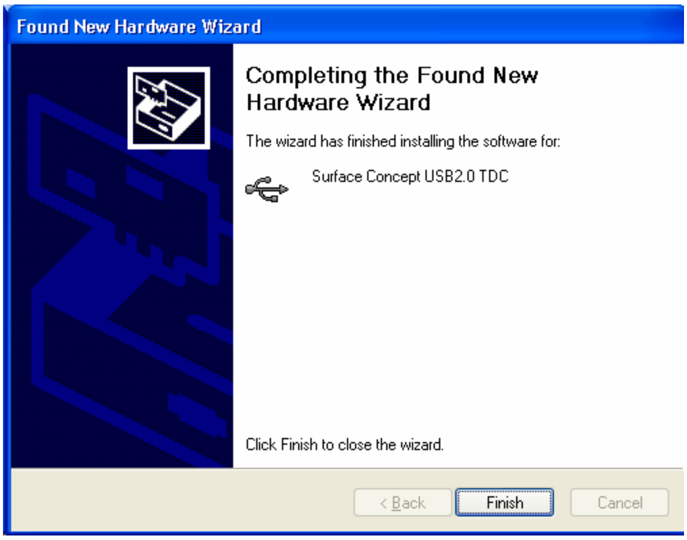
- Enter the path where the driver is located (or Browse to it)



- The internal name of the USB2.0 TDC driver is “ceusb3.sys”, select it and press “Open”.



- To continue, click "OK". The driver for the Surface Concept USB2.0 TDC will be installed.
- After a few seconds, a finishing dialog should appear as below. To finish, click "Finish".



Note: After finishing the installation routine for the first time, it will start again. Go through the routine again a second time completely. The driver installation will be complete only after the second installation. The driver has to be installed again, when the USB cable is connected to a different USB port on the PC than at the last installation. In this case the driver installation should start automatically.

5 DLD - Principle of operation

5.1 Basics of delayline detection

A delayline detector (DLD) consists of a microchannel plate array for pulse amplification and an in-vacuum readout unit consisting of a meander structured delayline (DLD anode). Each hit position is encoded by a fast data acquisition unit, which also may detect the hit time referenced to an external clock in repetitive (stroboscopic) experiments.

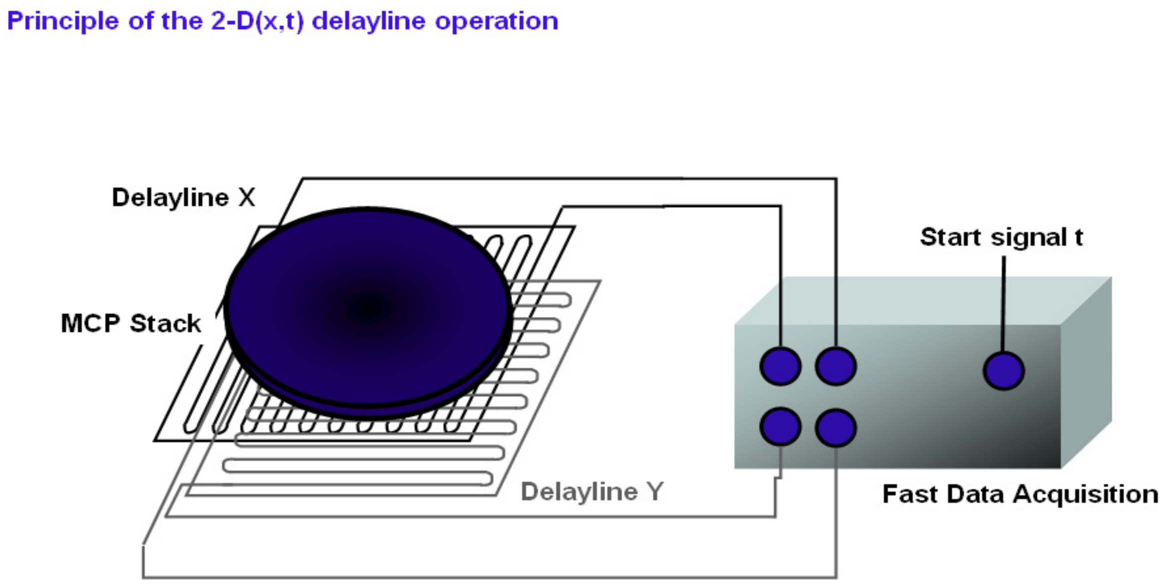


Figure 4: Schematic drawing of the basic assembly of a delayline detector

The DLD anode consists basically of two meander structured delaylines, the one rotated by 90° in respect to the other and both isolated from each other. The delaylines are positioned behind a Chevron microchannel plate stack, which is needed to amplify incoming electrons by at least 10^7. The electron cloud from the MCP stack output is drawn to the DLD meander (positive potential difference between anode and back side of MCP stack, defined by U_{DLD}) where it induces electrical pulses in the delayline by capacitive coupling. The pulses are traveling to the both ends of the meander within a time determined by the hitting position. The average time at both ends of the meander relative to an external repetitive clock generates the time coordinate if needed.

Delayline detectors are single counting devices; therefore the complete device works linearly even at extremely low numbers of incoming electrons.
The detection principle limits the maximum detectable count rates at least due to the maximum delay of the meanders. Currently, the main limitation is given by the appearance of multi-hit events, which can only be resolved up to a certain degree. The maximum count rate in the fourfold coincidence measurement is right now at about 2.0×10^6 counts per second.

5.2 Basic operational modes of the delayline detector

5.2.1 2D(x, y) area detection

The area detection mode is the normal operation mode of the delayline detector. The arrival times of pulses per event at the ends of the DLD coils are subtracted in order to determine a position in x and y (x: tx1-tx2; y: ty1-ty2). The 4 TDC stop signals are grouped internally in pairs to form x and y. All DLD software adjustments are done by the end-user software according to the user's chosen parameters.

5.2.2 3D(x, y, t) time resolved imaging

The delayline detector may measure all events in temporal reference to an external clock. For this mode, the user needs to start the USB2.0-TDC by an external clock, providing a low jitter LVTTL (or TTL) signal to the start input of the TDC.

Time measurements are performed by summing up the arrival times of pulses at the end of the DLD coils, i.e. the same results which are used to determine positions for each event are summed. It is possible to sum only tx1 and tx2 (tsumx) or ty1 and ty2 (tsumy). Because both sums should carry the same temporal information of a time related experiment, the total sum t(DLD) of all four time measurements (tx1, tx2, ty1, ty2) may be a good choice as well. The results of all this time sums correspond to t(sum) = t(offset) + n * (t(hit) – t(reference)), where (t(hit) – t(reference)) is the interesting time (e.g. ToF) in a given experiment, n is the number of summed time results (2 or 4 results), and t(offset) is a device immanent constant, which depends on cable lengths, electronics propagation times, experiments setup etc.. Therefore, it is possible to determine position and time of each event from only 4 precise time measurements completely.

The software may group all measured time sums in plain 1D time histograms, which are valid for the chosen region of interest (ROI). The time bin size for each readout channel x1, x2, y1 and y2 is 82ps in the normal resolution mode (I-mode, see chapter 8.2). The channel width in the 1D histogram is 41ps for the tsumx and tsumy histograms as well as 20.5ps for the total t(DLD) histogram.
The time bin size for the readout channels in the high resolution mode (R-mode, see chapter 8.2) is 27ps and the channel width in the 1D histogram is 13.5ps for the tsumx and tsumy histograms and 6.75ps for the total t(DLD) histogram. Due to the calculation of the tsums and t(DLD), the time axis is expanded virtually (simplified expression). The t(DLD) signature can be used in order to setup the regions of interest in time for measurements of time resolved images, the software is able to sample 3D histograms as image stacks in time, where each image corresponds to one time bin of the total time histogram.

5.3 Data acquisition

In the delayline detector, each coil/meander is connected to a fast amplifier followed by a constant fraction discriminator (CFD) for pulse shaping. They are encapsulated inside the pulse processing electronics (ACU = Amplifier-CFD-Unit or AU = Amplifier-Unit). The main function of the CFD is digital pulse discrimination, ideally without any time-walk even at varying pulse heights. A time-to-digital converter (TDC) behind these chains serves as stop-watch for arrival time measurements. The measurement results, in terms of differences and sums are fed into the PC via a USB 2.0 interface and are completed to 2D images (with or without time stamps) by the histogram module of the data acquisition DLL. Data processing and presentation on the PC is realized by the GUI software. See the corresponding software manuals for detailed information on the software package.

5.4 Working with the DLD – Important details

The DLD is a counting system that works laterally resolved by detecting four pulses from the four ends of the delayline coils in a fourfold coincidence. It only works correctly within a certain range of the supplying voltage. The MCP voltage has to exceed an operation threshold for the detector otherwise the pulse detection is not possible. This is due to the induced pulses on the delayline which have to reach a certain amplitude to be detected by the electronics, independent on the intensity of the electron source (e.g. mercury lamp). On the other hand, if the MCP voltage and/or the intensity of the electron source are too high, the detector overloads and again pulse detection is not possible. Saturation effects of the MCPs limit the amount of electrons provided by single pulses. An intensity increase of the electron source leads to an increased number of hits to the MCP. The current per bunch and therefore the amplitude of the pulses decreases. There are two kinds of overloads: local and global ones. A local overload (locally high intensity on the MCP) leads to no count rate within this local area and to an absolute “black spot” in the images. An intensity too high and homogeneously distributed over the whole MCP first leads to diffuse images and with further increasing intensity to randomly distributed artificial structures up to no count rate at all (global overload). The explanation for the effects for a local overload is a pulse amplitude that is too low to be detected by the electronics. The explanation for the global overload effects is mainly the loss of the fourfold coincidence condition of an incoming event and a fitting fourfold coincidence of random pulses, respectively. High intensity on the MCPs always leads to a significant pressure increase. Therefore an observed pressure increase can always be taken as an indicator for an overload of the detector, when problems with the functionality of the DLD occur.

Note: It is easy to mistake an overload for no signal at all. To distinguish between these two check the pressure. A pressure increase indicates an overload.

The DLD has been calibrated for an optimized MCP voltage and it is strongly advised to use this optimized voltage value for operation. It is given in the specification sheet and the commissioning sheet respectively. A change of the MCP voltage can lead to artifacts within the images. The MCP voltage should only be increased to compensate a decrease in amplification of the MCP stack do to wear out effects.

6 Delayline Detector Layout

6.1 Delayline detector - vacuum wiring

The delayline detector DLD 3030 consists of a rectangular detection area, defined by the detector cover and the MCP holders. The detector anode consists of two meander structured delaylines (named x and y), which are placed above each other (electrically isolated) and are orientated perpendicular to each other. The delayline in the top layer is referred to as the y meander and the delayline in the buried layer as the x meander. The x meander is orientated in the way to be sensitive along the dispersive direction. Figure 5 gives a schematic orientation of the x and y meanders,

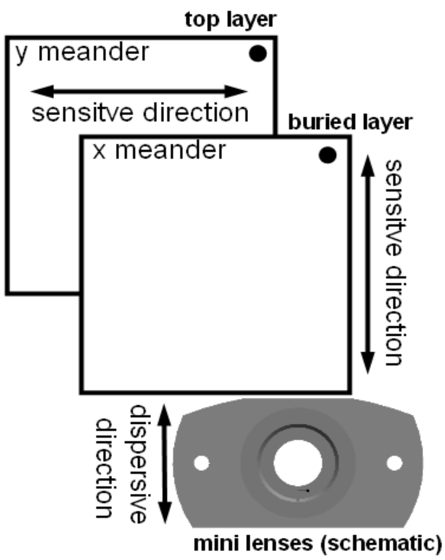


Figure 5: Schematic orientation and naming of the two meander-structured delaylines as well as the 0/0 position of the DLD image (black dot).

Signal readout is done via two readout lines (named 1 and 2) per meander structured. The naming of the four readout lines has been defined in the way, that the 0/0 position of a DLD image is positioned in the top right corner of the meander, when looking from the back side through the detector (see black dots in Figure 5). There are 4 readout lines in total for the complete detector. The naming of the single readout lines is put together of the individual naming 1 and 2 and the naming of the meander structured delayline x or y.

6.2 Delayline detector – connection ports

The delayline detector carries 2 CF 40 flange with each three single SHV feed-throughs for the high voltage supply of the detector and the mini lenses as well as a CF 40 flange, which holds 4 SMB feed-throughs for signal transfer (see Figure 6). The flange for the signal transfer also holds an orientation pin for correct orientation of the ACU. The allocation of the four signal channels X1, X2, Y1 and Y2 on the "SMB flange" can be taken from Figure 6.

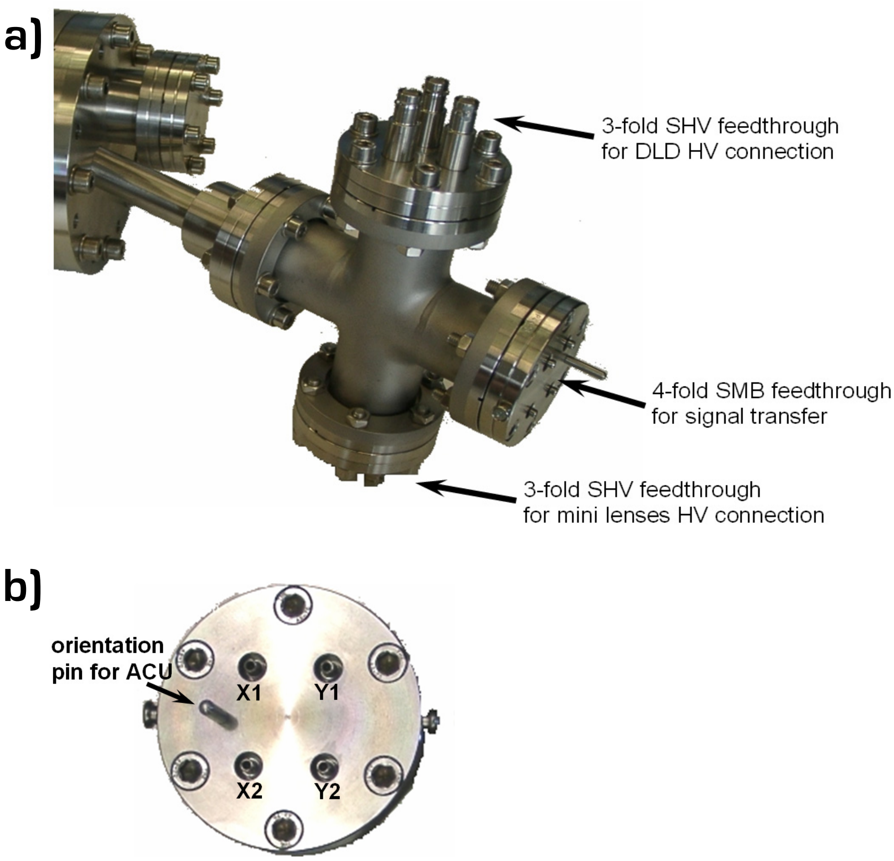


Figure 6: a) Connection ports for DLD 3030 with mini lenses, b) CF40 flange with 4-fold SMB feed-throughs in detail.

The high voltage potentials for the delayline detector: MCP front (F), MCP back (B) and anode (H) as well as for the mini lenses: front lens (LV), middle lens (LM) and back lens (LH) are written directly on the SHV feed-throughs. The internal high voltage connection for the delayline detector is given schematically in Figure 7.

<u>Note:</u> The resistance between MCP front and MCP back (resistance of MCP stack) should be in the range of 12 – 45 MΩ (the exact value is given in the specification sheet of your detector), while the resistance between MCP front and anode and MCP back and anode respectively should be unlimited.

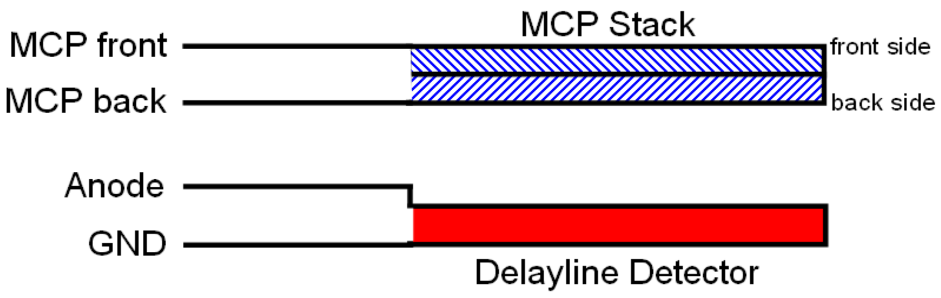


Figure 7: Internal connection of high voltage potentials (schematic)

Caution!

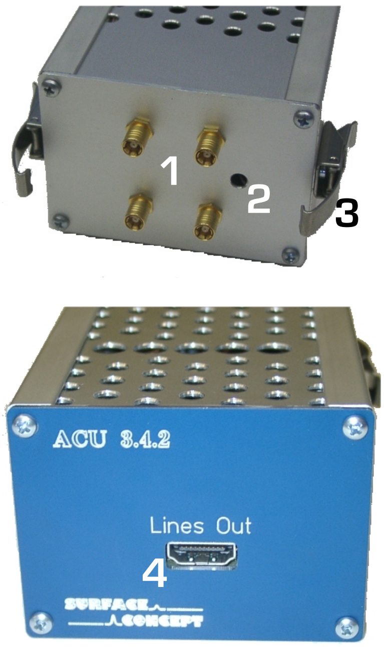
Do not disconnect single high voltage cables from the delayline detector as long as high voltage is applied. This will lead to high voltage sparks which can damage the very sensitive detector, the MCPs and/or the analogue readout electronics seriously.

7 Pulse processing electronics

The pulse processing electronics ACU (Amplifier-CFD-Unit) and AU (Amplifier-Unit) hold all devices like the amplifiers, pulse shapers, and constant fraction discriminators to turn the analogue pulses from the detector into digital pulses suitable for the Time-to-Digital Converter. Pulse decoupling is either realized within the pulse processing electronics or directly in-vacuum, depending on detector type and layout. Some pulse processing electronics also contain an integrated high voltage power supply for the complete detector. This also depends on the layout of the detector as well as the pulse processing electronics.

7.1 Pulse processing electronics ACU 3.4.2

The ACU 3.4.2 contains the amplifiers, pulse shapers and constant fraction discriminators.



1. 4x SMB sockets for signal transfer from SMB feedthrough
2. Hole for orientation pin from SMB feedthrough
3. Clip for fastening ACU to detector flange
4. Connection socket for DLD readout cable

Figure 8: Layout of ACU 3.4.2

The ACU can be plugged directly onto the 4-fold SMB feed-throughs. Fasten the two clips of the ACU to the fastening bolts of the CF 40 flange to fix it to the detector. Figure 8 shows the layout of the ACU 3.4.2.

Caution!

Do not disconnect the ACU 3.4.2 from the delayline detector as long as high voltage is applied. This can damage the analogue readout electronics.

7.1.1 Positions of the discriminator threshold regulators

Discriminator threshold regulators of the 4 DLD channels as well as a potentiometer for an additional adjustment of the amplification can be found on the corresponding boards inside the ACU 3.4.2. They can be reached through the holes on the top side of the ACU housing (see Figure 9).

The adjusting of the readout electronics goes hand in hand with the detector voltage. In fact there is only a small "window" for an optimum setting of the readout electronics for a given operation voltage. Changes of the detector voltage other than to compensate loss in the amplification of the MCP stack due to wear out effects, will lead directly to a loss in performance of the readout electronics (artifacts within the image, increased dark count rate etc.). The readout electronics is adjusted to its best performance to the operation voltage of the detector when delivered. A new adjustment should not be needed. The operation voltage is given in the specification sheet.

Note: The sensitivity of the CFD is increased (threshold decreased) by turning the screw of the potentiometer clockwise and vise versa for decreasing the sensitivity of the CFD. This is only to use when under some circumstances adjusting becomes necessary at all under.

Caution!

Do only adjust, if you have a real signal at the detector and a monitor for the results.

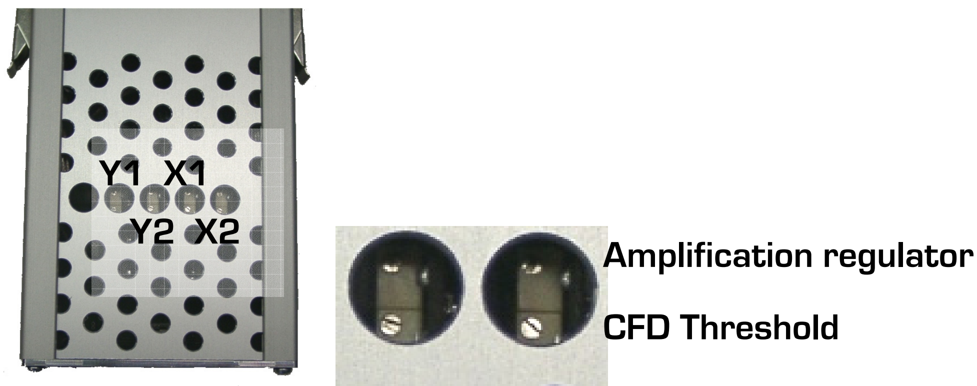


Figure 9: Labeling of discriminator threshold and amplification regulators.

8 Time-to-Digital-Converter (TDC)

8.1 Schematic description of the USB2.0-TDC

The USB2.0-TDC series combines the excellent performance of the GPX TDC chip (ACAM GmbH) with a high speed USB interface, either in the design with a single GPX chip (USB2.0-TDC) or with two GPX chips (Double USB2.0-TDC) operated in I-mode or in the high resolution design with two GPX chips operated in R-mode (High Resolution USB2.0-TDC). A special layout comes with the Dual Channel USB2.0-TDC. A TDC with one GPX chip operated in R-mode. This TDC is especially made for the readout of 1D(x)/2D(x,t) delayline detectors. It carries not only the TDC and FPGA electronics, but also the analogue readout electronics (pulse amplifier and constant-fraction-discriminators) for two signal lines.

A field programmable gate array (FPGA) enables comfortable setups and a variable data stream handling from the TDC via USB 2.0.
The main delayline detector and segment readout (optional device) functionality is permanently programmed. A complex FIFO design makes data losses almost impossible. The user DLL controls the data handling and streaming for the user. In this light, the following brief description about the internal structure of the measurement unit is only informative:

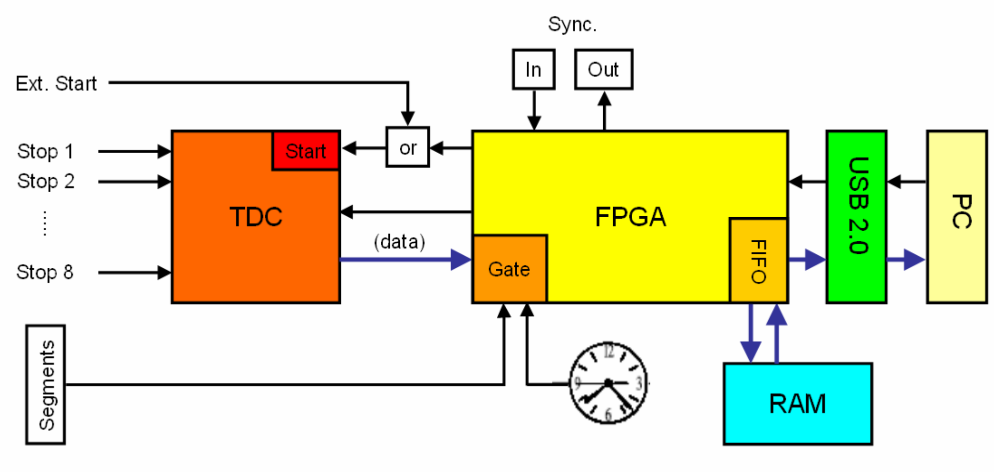


Figure 10: Schematic sketch of TDC functioning

Arrival times of pulses on the stop inputs are measured by the TDC in respect to either an internal reference start signal, provided by the FPGA, or an external start signal. Data from the segments are read out directly by the FPGA. The measurement dwell times for data from the TDC as well as from the segments are settled within the FPGA by a quartz stabilized time gate in an interval from 1 ms to 1193 h. The synchronization pulses for the external acquisition start (Sync. In) is fed directly into the FPGA, controlling the acquisition process. The FPGA also sends out the synchronization pulse for marking the end of an acquisition (Sync. Out). The TDC data streaming can be performed as measured (RawData mode) or including a DLD specific data pre-conditioning (Pair mode). This concerns a channel pairing and a pair result arithmetic, a modulo arithmetic and many more. Communication to and from the PC is realized via a USB 2.0 interface. Data streaming via the USB 2.0 interface is provided without losses using a large memory buffer within the device.

8.2 Basic operation modes of the GPX TDC chip

8.2.1 I-Mode (USB2.0-TDC/ Double USB2.0-TDC)

- 8 stop channels with typ. 81 ps digital time bin resolution
- 1 start channel
- Input level: TTL or LVTTL
- 5.5 ns pulse-pair resolution on one channel and 0 ns between two channels
- 32-fold multi-hit capability = 182 MHz peak rate
- Trigger to rising or falling edge
- Measurement range: 0 ns – 10.6 µs in start-stop operation
- Endless measurement range by internal retrigger of START
- 10 MHz continuous rate per channel
- 40 MHz continuous rate per chip

8.2.2 R-Mode (High Resolution USB2.0-TDC/ Dual Channel USB2.0-TDC)

- 2 stop channels with 27 ps digital time bin resolution
- 1 start channel
- Input level: differential LVPECL
- 5.5 ns pulse-pair resolution on one channel and 0 ns between two channels
- 32-fold multi-hit capability = 182 MHz peak rate
- Trigger to rising or falling edge
- Measurement range: 0 ns – 40 µs in start-stop operation
- 40 MHz continuous rate per channel
- 40 MHz continuous rate per chip

8.2.3 M-Mode (average mode – currently not implemented)

The M-mode is an internal averaging mode and needs very strict boundary conditions for operation.

- Time delay between stop and start pulse: > 130ps
- 2 stop channels with 10 ps digital time bin resolution (standard deviation, 70 ps peak-peak)
- 1 start channel
- Input level: differential LVPECL
- Single hit per Start and channel
- Trigger to rising or falling edge
- Measurement range: 0 ns - 10 µs
- Quiet Mode (no ALU operation and Data-output during measurements)
- Max. 500 kHz continuous rate per channel
- Max. 1 MHz continuous rate per chip

8.3 Layout of the High Resolution USB2.0-TDC

1. TDC Power socket
2. BNC sockets for trigger synchronization IN and OUT
3. HDMI socket for DLD readout cable from ACU
4. USB 2.0 connection socket
5. BNC socket for TDC start input
6. Power switch to turn the TDC ON/OFF. Lighted, when set to ON

Figure 11: Layout of the Double USB2.0-TDC

8.3.1 TDC Inputs (Stop + Start)

The USB2.0-TDC provides a HDMI socket for the signal input (stop inputs) from the ACU. The TDC inputs are laid out for PECL levels (R-mode operation mode).

An external start signal must be provided to the TDC for time resolved measurements. Apply standard TTL signals to the “TDC-start” input (BNC socket).

Note: The USB2.0-TDCs are not working with start signals of frequencies larger than 7 MHz. Therefore larger start pulse frequencies must be divided down with an appropriate frequency divider (e.g. divider with factor of 16 for 80 MHz start pulse frequency).

The temporal resolution is influenced mainly by the quality of the start signal while the TDC measures the time in a leading edge determination. Therefore, if the start signal is varying in time, one needs to process it by means of a constant-fraction-discriminator or similar external electronics components.

8.3.2 Trigger synchronization IN/OUT

Image acquisition of the DLD can be synchronized to an external trigger signal. To do so, the trigger signal must be applied as TTL signal to the “SYNC IN” BNC socket of the USB2.0-TDC. Additionally the corresponding software switch “ext_trigger” must be set to “1” in the delayline.dll. Otherwise the TDC ignores external trigger signals. The TDC provides a TTL signal on the “SYNC OUT” BNC socket after each acquisition. This function is always activated. No software switch must be set.

8.4 Interface (PC) and software

All operation functions of the USB2.0-TDCs for data readout of the detector package are encapsulated in the dynamic linked library “delayline.dll”. Data processing and presentation on the PC is realized by an end-user software (e.g. GUI, SpecsLab or Imspector). See the corresponding software manuals for detailed information on the software package and the DLL interface.

9 Operation of the DLD

9.1 Bake-out

Caution!

- **Please read the bake-out instruction completely and carefully, <u>before</u> starting the bake-out.**
- **Windows and feed-throughs should be wrapped with aluminum foil, to protect them from fast temperature changes.**
- **The use of heating tapes and jackets is not recommended, because of danger of local overheating.**
- **Do not remove the blankets until the entire system has thoroughly cooled off.**
- **Do not operate the detector before the temperature came back to ambient conditions.**
- **The detector electronics must be removed before any bakeout. Release the clips at the feed-through to remove the unit.**

Caution!

After a bakeout, the analyzer needs two days to cool down. If channel plates are operated at higher temperatures (> 50°C) they can suffer damage. Such channel plates will lose gain and exhibit a markedly higher detector plateau.

Even if the analyzer housing feels just warm, any internal parts seated on insulators may still be too hot for safe operation. It is imperative that all users be informed of this issue and take the necessary precaution to ensure proper device operation.

It is imperative that all users be informed of this issue and take the necessary precaution to ensure proper device operation.

9.2 Getting started

Be sure, that the vacuum pressure at the detector is remarkably below 10^{-6} mbar, otherwise the microchannel plates might be damaged by a local discharging. In general: as lower the pressure, as longer will be the lifetime of the MCPs.

Finish the complete cabling as described in chapter 3 before the TDC is turned on and the software is started.

Caution!

Turn off the high voltage, close the software and turn off the TDC before performing any changes of the cabling. This applies especially to the connection and disconnection of the:

- HV SHV cables (to prevent high voltage sparks)

- ACU 3.4.2

- start input of the TDC (the start input of the TDC cannot handle pulses which are arriving in a time interval of smaller than 150 ns, as they are produced by e.g. connecting to and disconnecting from the start input of the TDC respectively during operation)

9.3 High voltage turn on

Caution!

High voltage sparks may damage the very sensitive meander delaylines or the MCPs seriously. Observe the chamber pressure carefully every time the high voltage is turned on. Switch off the high voltage immediately in case of a temporary pressure rise by an order of magnitude or more.

9.3.1 “Start-Up” procedure

The first time the detector is used or after the system has been vented, the detector high voltages must be ramped very slowly to the final operation value. During this time the photon/electron source should not be operated. Details of how to ramp the voltage is given in Table 2.

Caution!

If sparking occurs, turn down the high voltage immediately, wait some time (up to 5 min.) and start the “Start-Up” procedure again with an increased ramp time. Is it not be possible to reach the operation voltage without sparking, then turn off the high voltage, stop the procedure and call SURFACE CONCEPT for further assistance.

MCP front actual	MCP front target	Anode actual	Anode target	MCP back actual	MCP back target	Ramp time
GND	GND	0 V	1000 V	0 V	1000 V	1000 s
GND	GND	1000 V	1700 V	1000 V	1700 V	1000 s
GND	GND	1700 V	1900 V	1700 V	1700 V	300 s

Table 2: Recommended “Start-Up” procedure for the detector voltages with MCP front to ground potential

<u>Note:</u> The final voltages for MCP back and detector anode given in Table 2 are just exemplarily. The analogue readout electronics has been adjusted to an optimized detector voltage. This voltage is given in the specification sheet of the detector. The detector voltage should only be increased to compensate loss in the gain of the MCPs due to wear out effects. The specification sheet also includes the number of

MCPs in your detector.

Caution!

Never exceed 2000 V in MCP back voltage when working with two MCPs and 3000 V when working with three MCPs respectively, in respect to the MCP front potential.

If the detector is operated with the MCP front potential set to a reference voltage other than the ground potential, than all three potentials (MCP front, MCP back and detector anode) should be ramped as given in Table 3.

MCP front actual	MCP front target	Anode actual	Anode target	MCP back actual	MCP back target	Ramp time
0 V	1000 V	0 V	1000 V	0 V	1000 V	1000 s
1000 V	2000 V	1000 V	2000 V	1000 V	2000 V	1200 s
2000 V	2000 V	2000 V	3000 V	2000 V	3000 V	1200 s
2000 V	2000 V	3000 V	3700 V	3000 V	3700 V	1000 s
2000 V	2000 V	3700 V	3900 V	3700 V	3700 V	300 s

Table 3: Recommended "Start-Up" procedure for the detector voltages with MCP front on a reference potential other than ground.

Check the detector output by means of the used software. The dark count rate without any source should be lower then 50 cps at the entire active detector area.

Now you may start carefully with an electron source observing the detector output.

Note: Keep in mind the description about the important operation details in chapter 5.4.

9.3.2 Standard start procedure

The following procedure is used for all later operation starts, when the detector has already been operated in vacuum and has not been vented in between:

Turn off all electron sources to avoid overloads at the detector during the start of operation. Turn on the voltages slowly; turn stepwise within 2 or 3 minutes to the operation voltages of MCP front, MCP back and the detector anode.

Watch the vacuum pressure during this procedure; turn the voltages back, if an unusual increase is observed in the pressure.

Check the detector output by means of the used software. The dark count rate without any source should be lower then 50 cps at the entire active detector area.

Now you may start carefully with an electron source observing the detector output.

<u>Note:</u> Keep in mind the description about the important operation details in chapter 5.4

9.4 Getting started

Caution!

Be sure that the vacuum pressure in the detector is safely below 10^{-6} mbar, otherwise the microchannel plates might be damaged by local discharging. In general: the lower the pressure, the longer the lifetime of the MCPs will be.

Place the ACU 3.4.2 to the 4-fold SMB feed-through and fix it with the clips to the bolds on the CF40 SMB flange. Finish the cabling as described in chapter 3.2.2.

Turn on the TDC and start the GUI software.

9.5 Special operation modes of the delayline detector

Additionally to the basic operation modes of the delayline detector as described in chapter 5.2, the following special operation modes exist:

9.5.1 Virtual segmented anode

A virtual exit slit size can be varied freely down to 100 µm using the delayline readout system. This mode is optional and currently not implemented in the front-end software.

9.5.2 3D temporal imaging

The delayline detector can measure all events in respect to time with an external clock. For this mode, the user needs to start the USB2.0-TDC by an external clock, providing a low jitter LVTTL signal to the start input of the TDC. The temporal resolution may be influenced mainly by the quality of this signal while the TDC measures the time of it with the leading edge of this signal. Therefore, if this reference signal is varying in time, one needs to process it by means of a constant-fraction-discriminator or similar external electronic components.

10 Microchannel plate

<u>Note:</u> Contact SURFACE CONCEPT before performing a replacement.

Take care to note the orientation of the MCPs. The channels in the MCPs include an angle of 8° against the surface normal of the plate and the MCP's must be mounted in a chevron configuration. All parts of the detector, especially the MCPs should be handled with great care. The MCP surfaces are very sensitive and should never be touched or scratched.

10.1 Storage

Because of their structure and the nature of the materials used in manufacture, care must be taken when handling or operating MCPs. The following precautions are strongly recommended:

- The most effective long-term storage environment for an MCP is an oil free vacuum.

10.2 Handling

- Shipping containers should be opened only under class 100 Laminar flow cleanroom conditions.
- Personnel should always wear clean, talc-free, class 100 clean-room compatible, vinyl gloves when handling MCPs. No physical object should come into contact with the active area of the wafer. The MCP should be handled by its rims, there is no solid glass border! Use clean degassed tools fabricated from stainless steel, Teflon™ or other ultra-high vacuum-compatible materials. Handling MCPs should be limited to trained, experienced personnel.
- MCPs without solid glass border should be handled very carefully with great care taken to contact the outer edges of the plate only.
- The MCP should be protected from exposure to particle contamination. Particles which become affixed to the plate can be removed by using a very pure and low pressure air flow such as from a clean rubber bellows.
- The MCP should be mounted only in fixtures designed for this purpose. Careful note should be taken of electrical potentials involved.

Caution!

Voltages must not be applied to the device while at atmospheric pressure. The pressure should be 1 x 10^{-6} mbar or lower at the microchannel plate before applying voltage. Otherwise, damaging ion feedback or electrical breakdown will occur.

10.3 Operation

- A dry-pumped or well-trapped/diffusion-pumped operating environment is desirable. A poor vacuum environment will most likely shorten MCP life or change MCP operating characteristics.
- A pressure of 1 x 10^{-6} mbar or better is preferred. Higher pressure can result in high background noise due to ion feedback.
- When a satisfactory vacuum has been achieved, voltages may be applied. It is recommended that this is done slowly and carefully. If fluctuations do appear, damage or contamination should be suspected and the voltage should be turned off. The assembly should then be inspected before proceeding.
- Voltage across single MCPs should not exceed 1000 volts. Higher potentials may result in irreversible damage.
- MCP's can be degraded by exposure to various types of hydrocarbon materials which raise the work function of the surface, causing gain degradation.
- Operation at higher temperatures (> 50 °C) will cause gain degradation.

Thickness	1.0 mm
Outer diameter	50 mm
Active diameter	46 mm
L/D (channel length / channel diameter)	40 : 1
Resistance (single MCP)	3 – 13 MOhms
Max. voltage (single MCP)	1000 V
Max. Gain @ 1000 V (z-stack)	$\geq 1 \cdot 10^{8}$ minimum
Pulse height dist. (z-stack)	100 %
Pore size (diameter)	25 µm
Center – to – Center Spacing	32 µm
Bias angle of channels	8° ± 1°
Quality level	detection quality, z-stack matched, extended dynamic range
Open area ratio	45 % minimum
Operating pressure	$< 1 \cdot 10^{-6}$ mbar

Table 4: MCP Specifications

11 Technical Data

Delayline detector general:

Active area of each quadrant:	30 mm x 30 mm
MCP size:	50 mm OD, 25 µm pore size, L/D = 40:1, amplification of chevron stack at about 10^8
Max. voltage at detector:	1.0 kV per MCP in MCP stack
Max. voltage at MCP front:	1.0 kV
Max. voltage difference between U_{DLD} and CH-HV:	900 V (typ. 400 V)
Max. bake-out temperature:	150°C
Vacuum pressure range for operation:	< 10^{-6} mbar

Amplifier – CFD – Unit ACU 4.4:

Bandwidth of DLD amplifiers:	1.6 GHz
CFD working frequency:	200 MHz
CFD jitter (max.):	20ps
CFD walk (typ.):	< 50 ps (while ambient temperature varies less then 5 K)

USB2.0-TDC (One GPX chip):

- Low voltage TTL inputs, common start input usable as reset of the internal clock resolution adjust mode: quartz-accurate, adjustable resolution, insensitive to temperature variations, adjustable via software (no calibration necessary)
- 8 stop channels with typ. 81 ps digital time bin resolution
- 1 start channel
- Start retrigger rate (max): 7 MHz
- Measurement range 0 ns – 10.6 µs in start-stop operation
- Dynamic range: 2^{17}
- Trigger to rising or falling edge
- Endless measurement range by internal retrigger of START
- All channels provide precisely an equal resolution
- No minimum time limit for hits at different channels
- 5.5 ns pulse-pair resolution on one channel and 0 ns between two channels
- 32-fold multi-hit capability = 182 MHz peak rate
- 40 MHz internal rate
- Max. data acquisition rate of 2.5 MHz
- Counter line frequency limit of 35 MHz per channel

Double USB2.0-TDC (Two GPX chips):

- Low voltage TTL inputs, common start input usable as reset of the internal clock resolution adjust mode: quartz-accurate, adjustable resolution, insensitive to temperature variations, adjustable via

software (no calibration necessary)
- 16 stop channels with typ. 81 ps digital time bin resolution
- 2 start channels
- Start retrigger rate (max): 7 MHz
- Measurement range 0 ns – 10.6 µs in start-stop operation
- Dynamic range: 2^{17}
- Trigger to rising or falling edge
- Endless measurement range by internal retrigger of START
- All channels provide precisely an equal resolution
- No minimum time limit for hits at different channels
- 5.5 ns pulse-pair resolution on one channel and 0 ns between two channels
- 32-fold multi-hit capability = 182 MHz peak rate
- 40 MHz internal rate
- Max. data acquisition rate of 2.5 MHz
- Counter line frequency limit of 35 MHz per channel

High Resolution USB2.0-TDC (Two GPX chips):
- Differential PECL (LVPECL) inputs, common start input usable as reset of the internal clock resolution adjust mode: quartz-accurate, adjustable resolution, insensitive to temperature variations, adjustable via software (no calibration necessary)
- 4 stop channels with 27 ps digital time bin resolution
- 1 start channel
- Start retrigger rate (max): 9 MHz
- Measurement range 0 ns – 40 µs in start-stop operation
- Dynamic range: 2^{19}
- Trigger to rising or falling edge
- All channels provide precisely an equal resolution
- No minimum time limit for hits at different channels
- 5.5 ns pulse-pair resolution on one channel and 0 ns between two channels
- 32-fold multi-hit capability = 182 MHz peak rate
- 40 MHz internal rate
- Max. data acquisition rate of 2.5 MHz
- Counter line frequency limit of 35 MHz per channel

12 List of Figure

EU Declaration of Conformity 2008

Manufacturer **Surface Concept GmbH**
Staudinger Weg 7
D - 55128 Mainz
Germany

CE

Product details Delayline Detector DLD 3030 to be operated with ACU 3.4.2, and USB2.0-TDC.

The above named product comply with the following European directive:

89/336/EEC	Electromagnetic Compatibility Directive, amended by 91/263/ EEC and 92/31/ EEC and 93/68/EEC
73/23/EEC	Low Voltage Equipment Directive, amended by 93/68/EEC

The compliance of the above named product to which this declaration relates are in conformity with the following standards or other normative documents where relevant:

EN 50081-1 (3/94)	Electromagnetic Compatibility Generic Emission Standard-Part 1:
EN50082-1 (3/94)	Electromagnetic Compatibility
EN 61010-1 (2001)	Safety Requirements for Electrical Equipment for Measurement, Control and Laboratory Use

Issued on 01. June 2008

For and on behalf of **Surface Concept GmbH**

Mainz, 01.07.2008 (date)

Legal signature .... (Dr. Andreas Oelsner – Managing Director)

This declaration does not represent a commitment to features or capabilities of the instrument. The safety notes and regulations given in the product related documentation must be observed at all times.

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