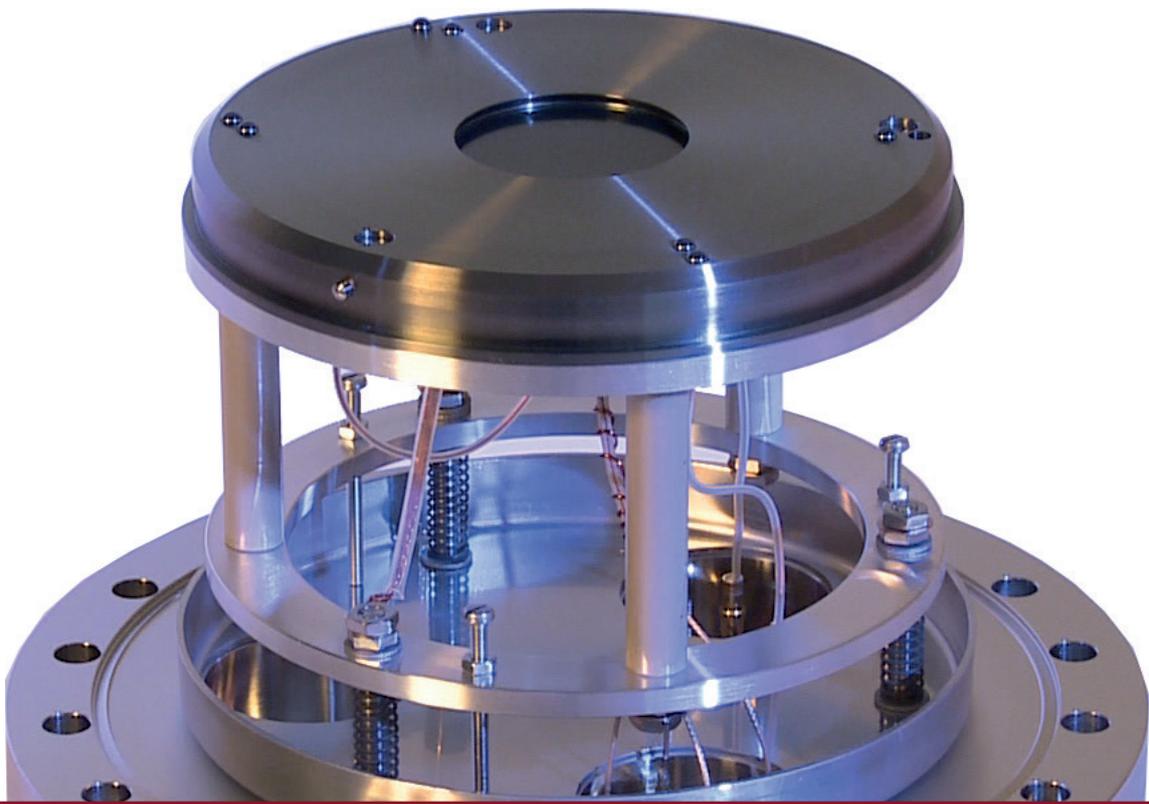


# Delayline Detectors

Imaging Detection of Electrons, Ions & Photons  
with Picosecond Time Resolution

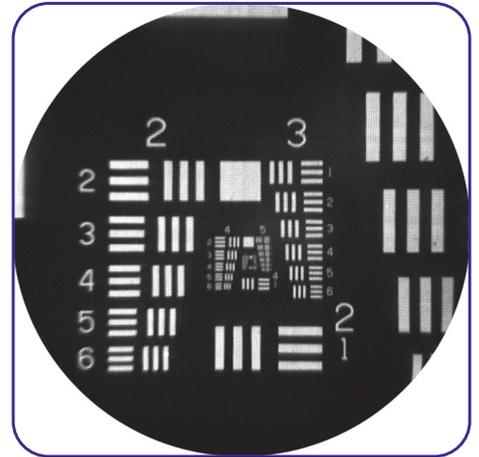


# 3D Detector Systems

## - Imaging Detectors with Time Resolution -

Boost your particle analysis to a new level of high speed measurement. Delayline Detectors are superior particle imagers with excellent temporal resolution, very fast sampling (up to several 10MHz), and 1D/2D/3D histogramming on the fly.

Anyone who aims for permanent, dead time free data streaming will largely benefit from the use of our multidimensional detector layouts.



Imaging of a UV-irradiated USAF 1951 type mask with a 40mm DLD



Delayline Detector DLD4040 R2.55 with 40mm active area

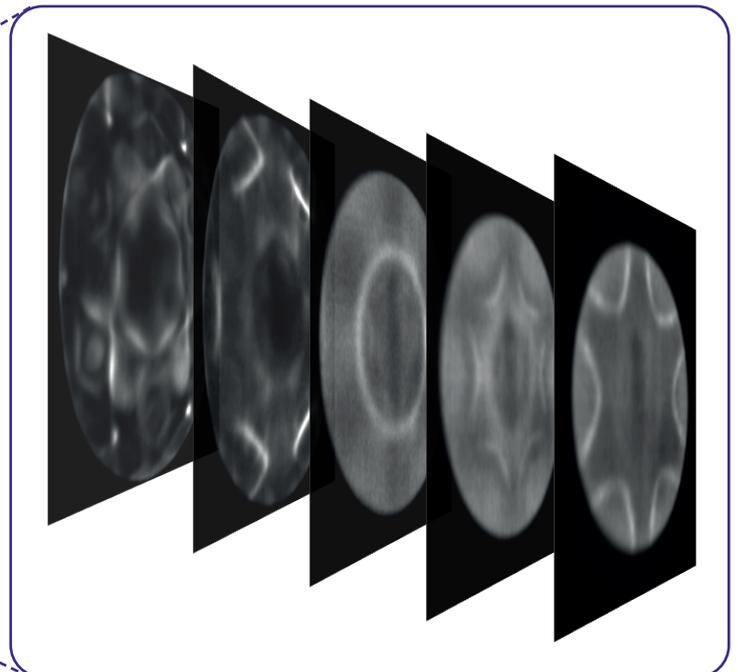
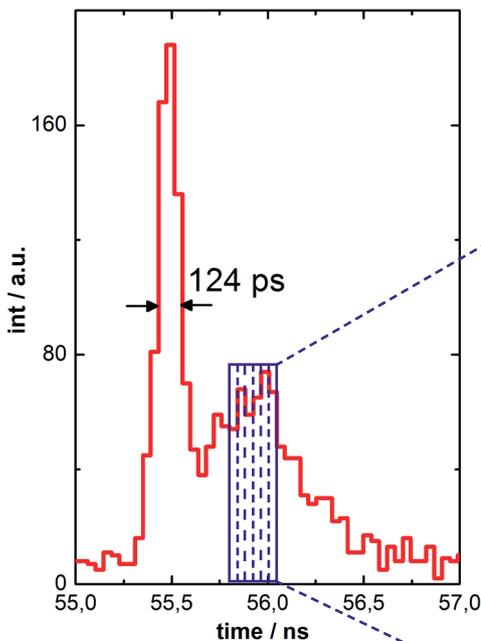


Image time slices measured with a DLD

# Delayline Detector Package - Accompanying Readout Electronics -

Our Delayline Detectors do not come as pure vacuum heads but as a complete detector package with accompanying readout electronics of analogue pre-amplifier and constant-fraction discriminator unit (ACU) and time-to-digital converter (TDC) adjusted among each other for the best possible performance of the detector. The package also contains our GUI demo software for detector readout and data saving and additionally on request a high voltage power supply with floating capability.

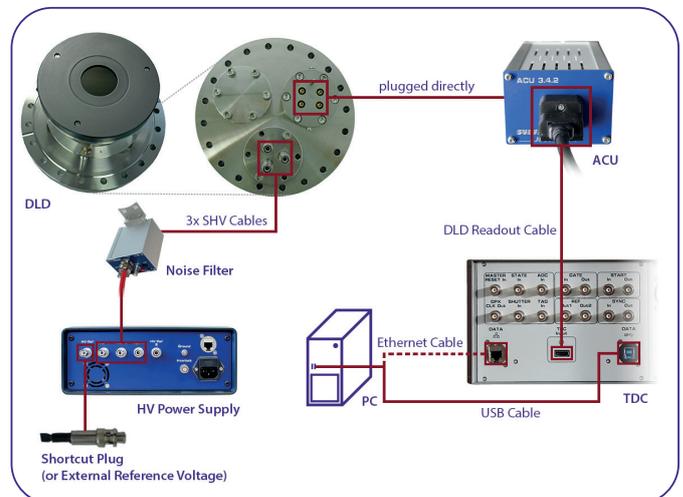


4-channel pre-amplifier and constant-fraction discriminator unit (ACU)

4-channel time-to-digital converter (TDC) with two interfaces (USB3.0 and 1Gbit Ethernet) and with extended I/Os for advanced measurement applications (like ADC input, counter input, gate input and output).

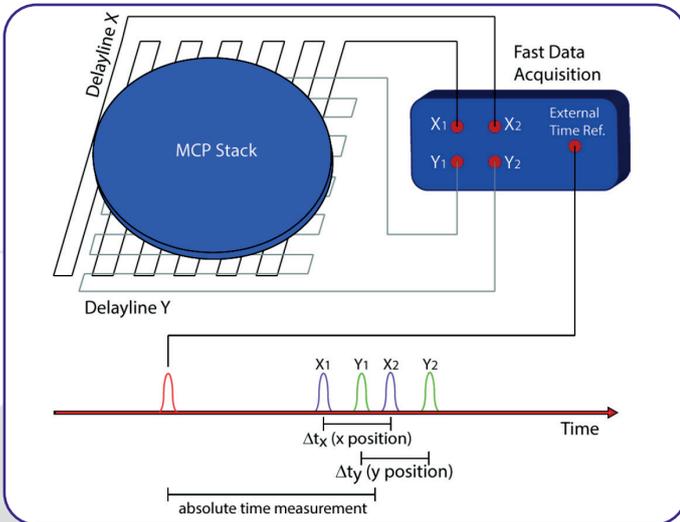


3-channel noise filter with integrated voltage limiter to protect the MCPs and the detector anode from overvoltage.



Cabling scheme of a Delayline Detector package.

# Delayline Readout of MCPs - The Technical Approach -



Microchannel-Plate (MCP) detectors provide the **highest performance** in imaging of electrons, ions, neutrons and photons.

In case the application requires single event analysis, the delayline readout of MCPs is by far the best choice as the Delayline Detector (DLD) enables **true single event counting** with excellent signal-to-noise ratio and the **highest time resolution**.

Delayline readouts are superior among all time resolving MCP readout systems because they deliver **time slice images** with time windowing down to below 100ps with highest intensity linearity.

Operation principle of a DLD. Charge cloud coupling from an MCP stack into an anode structure delayline arrangement enables the measurement of impact position and time by determining the arrival times of the pulses at the ends of the delaylines.

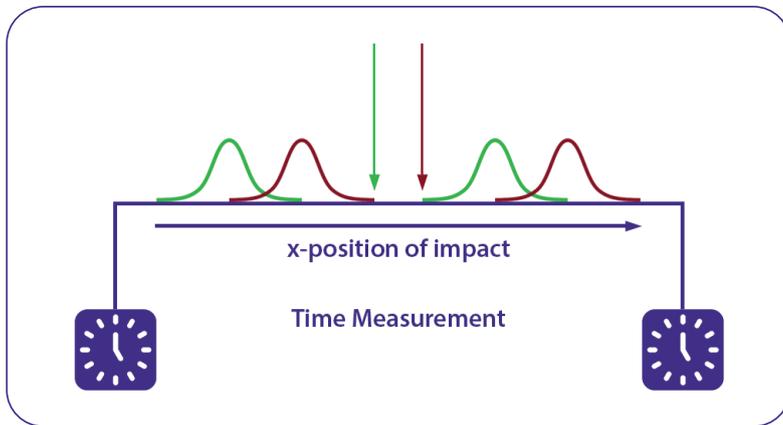
## Key Features

Active Diameters	10mm - 120mm
Lateral Resolution	down to 50µm
Imaging Countrate (Permanent Random)	> 5 million counts/s
Imaging Countrate (Special Layouts)	> 20 million counts/s
Max. Burst Rate	up to 100 million counts/s equivalent
Multi-Hit Designs	>= 4 hits
High Voltage Floating Capability	up to 10kV
Time Bin Resolution	6.8ps
Typical Time Resolution	< 85ps (RMS)
Start Repetition Rate	max. 9MHz
Data Interfaces	USB 3.0 & Gbit LAN



Customer specific solution of a Delayline Detector design

# Segmented Anodes - For Improved Multi-Hit Detection -

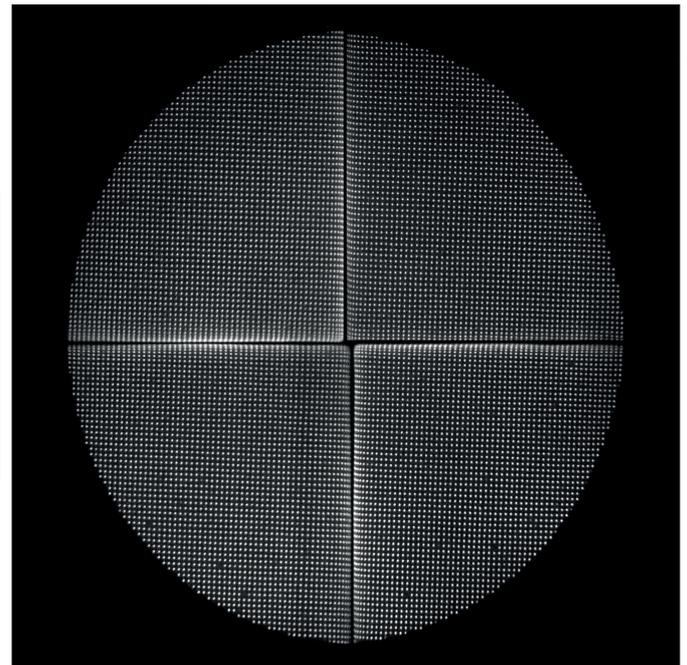


Delayline Detectors feature only a limited **multi-hit capability** due to their event-counting working principle. Two events at the same position and the same time cannot be clearly distinguished.

Therefore Surface Concept provides different types of segmented Delayline Detector anodes (like in 4 quadrants, 8 segments or customer specific segmentation) to improve the **multi-hit capability**.



4-fold segmented DLD with 80mm active area



Detector image of a shadow mask recorded with a 4-fold segmented DLD showing the segmentation of the detector anode

## Multi-Hit Concepts

Extensive multi-hit capability for novel applications like free-electron laser science is reached with the **Multi-Line Delayline Detector** by massive parallel segmentation of anodes perpendicular to the image plane with up to **256 single delaylines** which increases the number of detectable multi-hits to several tens.

# Applications

- Time-of-Flight Analysis of Electrons and Ions (ToF)
- Time Correlated or Coincidence Photon and Particle Imaging
- Gated Imaging for X-Ray and Electron Spectroscopy
- True Counting Imaging with large Areas up to 120mm Detection Size
- Electron Energy and Time-of-Flight Analyzers (XPS, UPS, EELS)
- Time-of-Flight Photoemission Electron Microscopy (ToF PEEM)
- Medium Energy Ion Scattering with Time-of-Flight Analysis (MEIS ToF)
- Atom Probe Tomography / Microscopy (APT, 3D-AP)
- X-Ray Absorption / Emission Spectroscopy (XAS, XES)
- X-Ray Picosecond Imaging by Means of Time Gating for Contrast Enhancement
- Fluorescence Lifetime Imaging (FLIM, FLIM-FRET)



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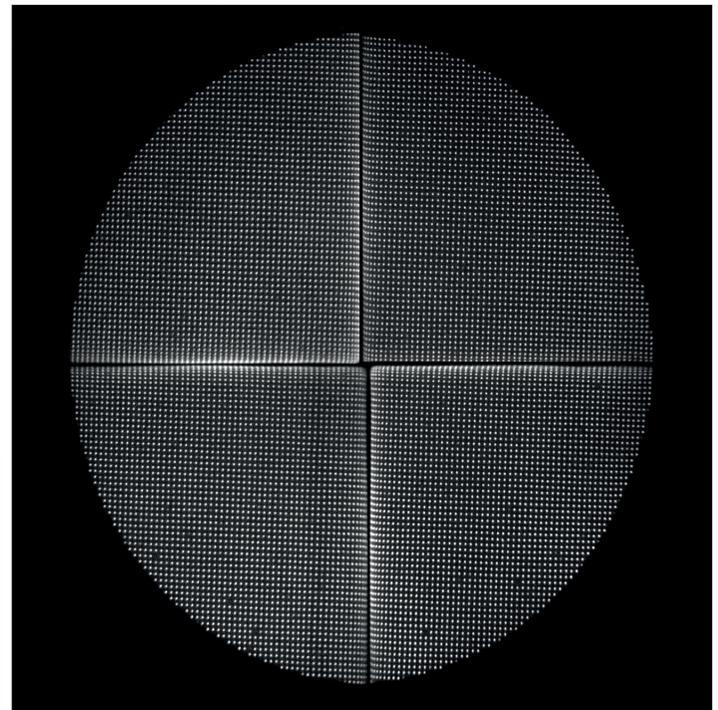
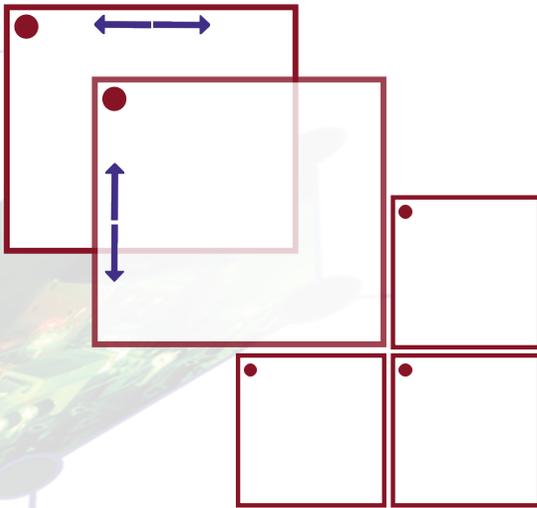
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**SURFACE** .....  
..... **CONCEPT**

# Segmented Anode Delayline Detectors - Layouts for Increased Multi-Hit Capability -

## DLD-4Q

Four fully independent quadrants provide at least 4 times greater multi-hit capability under uniform illumination.



Detector image of a shadow mask recorded with a 4-fold segmented DLD showing the segmentation of the detector anode.

## Key Features

Flange mounted, MCP based segmented Delayline Anode Detectors

With 3-fold SHV and 4x 4-fold SMB Feedthroughs

Active Area in Diameter 60mm, 80mm, 120mm

Pixel No. 1200x1200, 2100x2100, 4700x4700

Time Resolution  $\leq 100\text{ps}$  (RMS)

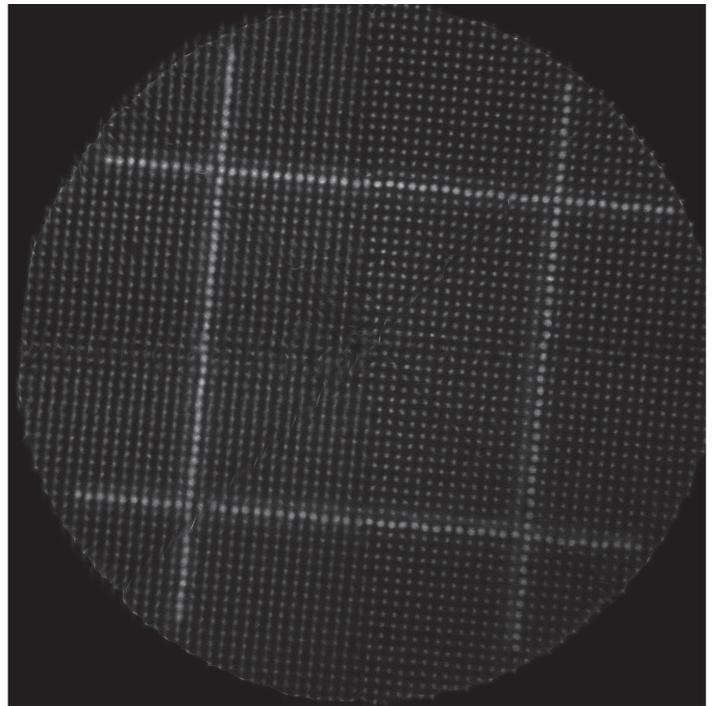
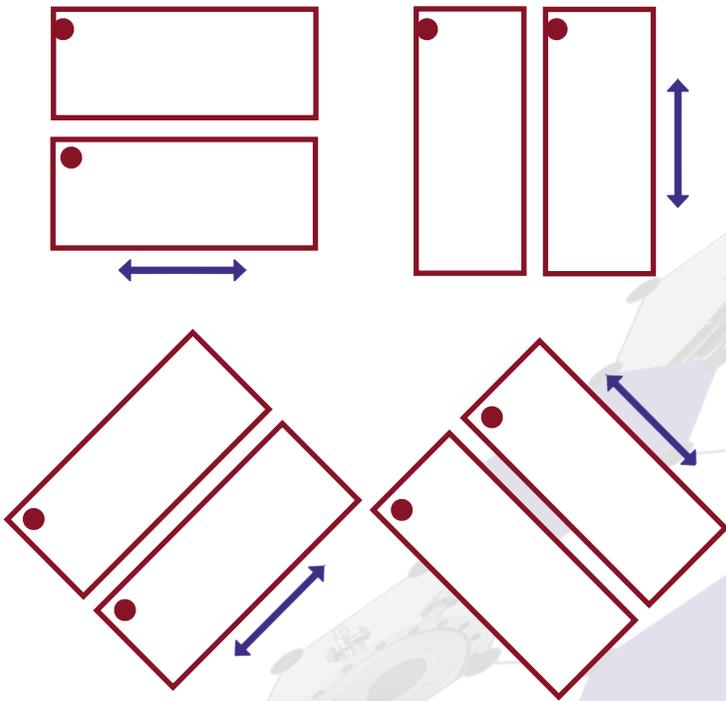
Max. Random Count Rate  $\geq 5\text{Mcps}$



# Segmented Anode Delayline Detectors - Layouts for Increased Multi-Hit Capability -

## DLD-85

Eight segments with partial overlap ensure the absence of “dead” areas and enhance multi-hit capability (two systems, one rotated 45 degrees relative to the other).



Detector image of a shadow mask with a structure recorded with a DLD-85 showing absence of “dead” areas.

## Key Features

Flange mounted, MCP based segmented Delayline Anode Detectors

With 3-fold SHV and 4x 4-fold SMB Feedthroughs

Active Area in Diameter

60mm, 80mm, 120mm

Pixel No.

1200x1200, 2100x2100, 4700x4700

Time Resolution

$\leq 100\text{ps (RMS)}$

Max. Random Count Rate

$\geq 5\text{Mcps}$



# NEW QUAD CHANNEL TDC R071

Time-to-Digital Converter for  
Delayline Detector Readout

**TIME RANGE UNLIMITED**

Extended Measurement Range Mode  
Overcome Intrinsic Limitation  
Allowing Virtual Unlimited Time Range



## New Features

- Data Interface: USB3.0 and 1Gbit Ethernet (selectable)
- Extended Measurement Range: Up to 27.4ps x 64bit (>5,000d)
- Additional Input for ADC, Tag, State, Shutter, Master Reset
- Reference Norm Pulse Outputs (LVTTTL)



# Technical Specifications

- 19" 3HE Rack Mount Housing
- Number of Stop Inputs: 4
- Number of Start Inputs: 1 (common start input usable as reset of the internal clock resolution adjust mode: quartz-accurate, adjustable resolution, insensitive to temperature variations, adjustable via software, no calibration necessary)
- Digital Time Bin Resolution per Channel: 27.4ps
- 5.5ns Pulse-Pair Resolution on one Channel and Ons between two Channels
- Trigger to rising Edge
- Start Retrigger Rate (max): 9MHz
- Measurement Range: Ons – 40 $\mu$ s in Start-Stop Operation (measurement range of 40 $\mu$ s corresponds to a start frequency of 25kHz)
- Measurement Range: 25 $\mu$ s – virtual unlimited (27.4ps \* 64bit) in extended measurement range
- Internal Start Frequency Divider (2-, 4-, 8-, 16- and 32-fold divider)
- Dynamic Range: 2E19
- All Channels provide precisely and equal Resolution
- 32-fold Multi-Hit Capability per Channel
- 80MHz Internal Device Measurement Rate
- Stop Signal Input: Low Voltage PECL (differential signal) on Differential Multiline Connector (adapted to connector layout of ACU of the detector head)
- External Start Signal Input: Low Voltage TTL on 500hm BNC Socket
- External Start Signal Output: Low Voltage TTL on BNC Socket
- Device Synchronization Signal Input: Low Voltage TTL on 500hm BNC Socket
- Device Synchronization Signal Output: Low Voltage TTL on BNC Socket
- Device Gate Signal Input: Low Voltage TTL on 500hm BNC Socket
- Device Gate Signal Output: Low Voltage TTL on BNC Socket
- Tag, State, Shutter and Master Reset Input: Low Voltage TTL on 500hm BNC Socket
- TDC Clk Signal, Ref Out 1 and Ref Out 2 Signal Output: Low Voltage TTL on BNC Socket
- ADC Input: 16bit ADC Input (+/-10V) on BNC Socket
- USB and Ethernet Interface for Data Transfer