Guidelines for efficient usage of imaging and time resolved imaging with Surface Concept Delay Line Detectors

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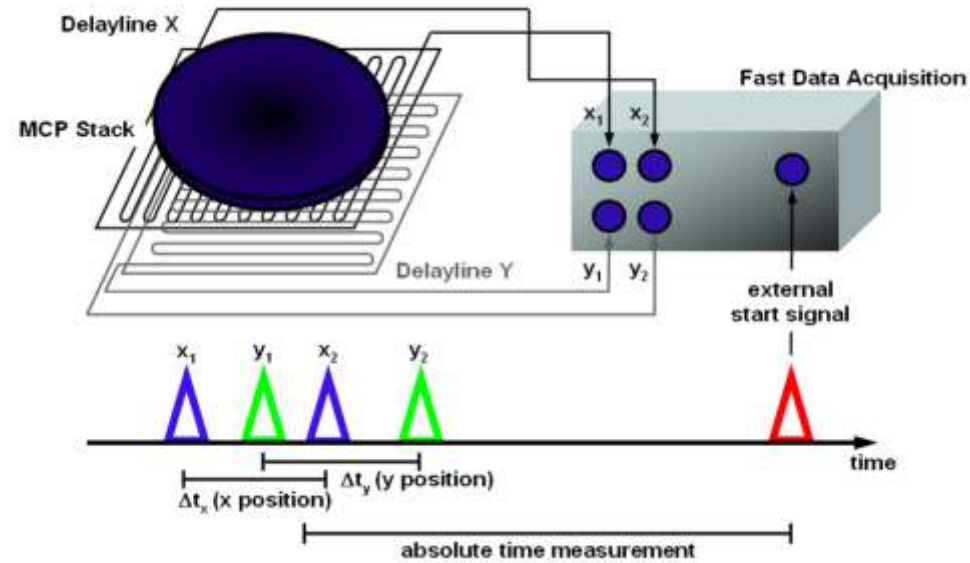www.surface-concept.de; oelsner@surface-concept.de

A delay line detector (DLD) is a position (x, y) and time (t) sensitive microchannel plate area detector for imaging of single counted particles with or without temporal resolution in the pico-second range.

The (x, y, t) histograms are gathered over very many excitation cycles of the particle generating process as the system is a single counting device. Particle images can be collected from continuous running processes with randomly incoming particle sequences without time correlation as well.

The dead time of these single counting devices are as small as 10 ns – 20 ns, which enables even live imaging with highest sensitivity, collecting high count rates of randomly incoming particles in the millions counts per second range, as well as imaging with a very high dynamic range of 10^6.

Unlike for other pico-second imagers, delay line detectors collect all incoming particle hits continuously without any gate window duty cycles, thus (besides the device dead time limits) all hits are collected even when they represent random time positions within the excitation cycle time period.

1. The data acquisition system measures 4 time values: x1, x2, y1, y2 for each incoming single event (an event corresponds to a single detected particle hit at any position at the detector's active area).

2. The reference time for all the time measurements is defined by an external start signal. That signal can be provided by the user from outside the acquisition unit or the system may generate it internally.

3. Image coordinates of each event are calculated by the difference times x = x1 - x2 and y = y1 - y2. The image coordinates x, y can be determined even when the start signal is not correlated to the detector hits.

4. Time coordinates t of each event are calculated by the sum of all 4 measured times from the single event data: t = x1 + x2 + y1 + y2. Useful time coordinate measurements require an appropriate correlation between the start signal and the incoming events. For that, the user must provide the start signal from outside.

5. Images – 2D (x, y) or 3D (x, y, t) – are formed by counting the histogram's memory cells belonging to the measured coordinates up by 1 for each measured single event. Acquisition of image histograms usually requires very many cycles of start-stop measurements.

6. The unit can detect numerous multiple hits after each start signal, but the minimum time distance between single hits is limited to 10 ns – 20 ns.

7. The start signal period must be above 140 ns.

The main time measuring unit is a Time-to-Digital Converter (TDC), different Surface Concept DLDs may use different types of TDCs.
Time range limits of the main types of used TDCs:

USB2.0-TDC (SMB input ports):
- max. start signal frequency: 7 MHz
- time coordinate spacing: 20.576148 ps
- max. measurement range between start and stops: 10.7 µs

Quad channel USB2.0-TDC (compact differential plug input):
- max. start signal frequency: 7 MHz
- time coordinate spacing: 6.858716 ps (G-mode*: 5.144037 ps)
- max. measurement range between start and stops: 40 µs (G-mode*: 64 µs)

* G-mode is used in singular detector systems, check your individual settings and data sheets of your detector
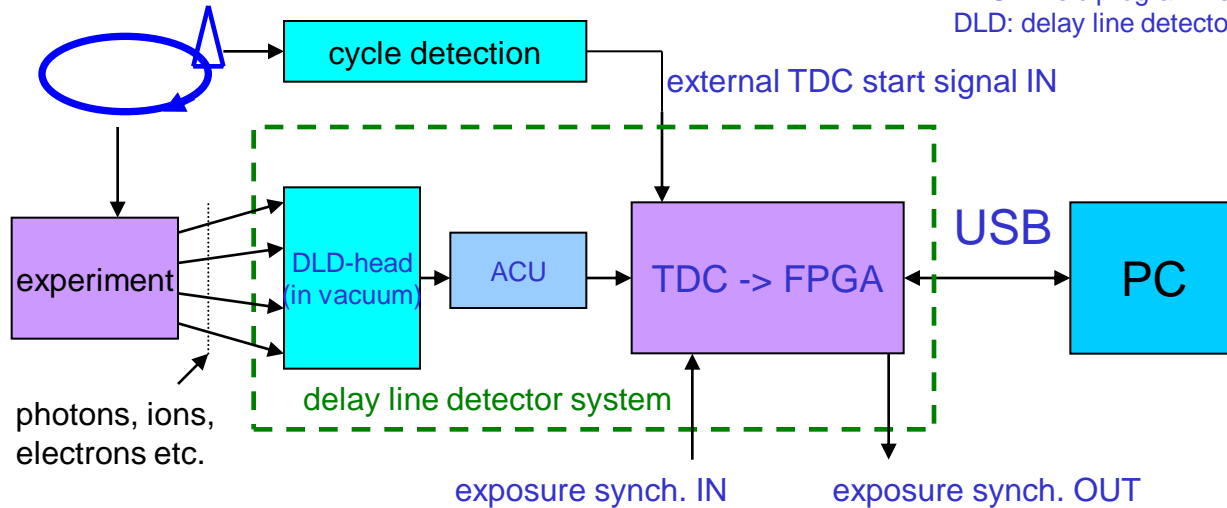
SURFACE CONCEPT

ACU: fast pulse processing electronics
TDC: time-to-digital converter
FPGA: field programmable gate array
DLD: delay line detector for subsequent single particle detection (x,y,t)

Cyclic running excitation source

cycle detection

external TDC start signal IN

experiment

DLD-head (in vacuum)

ACU

TDC -> FPGA

USB

PC

delay line detector system

photons, ions, electrons etc.

exposure synch. IN   exposure synch. OUT

On the PC:
- event coordinates (x, y, t) are counted up into 2- or 3-dimensional histograms building an image or a stack of (x, y) images for different times t. For 3D, the time t should be measured with respect to the "external TDC start signal".

- The time duration for event data collection is called an "exposure run" and spans usually over very many cycles of excitation.

- Exposure runs are in general not and do not need to be synchronized with the source cycles.

- 2D-histograming, i.e. (x, y) single imaging, is also possible, therefore the external start signal can stay unused and the excitation source may work in a cyclic or in a continuous mode.

Exposure functionality:
- Any measurement (or exposure run) starts when the FPGA is ordered from the PC application to measure and to send data for collecting a new image histogram or time resolved image stack within a well defined measurement dwell time. Live 3D image frame rates can reach 5 3D-frames per second.

- The exposure run start can be specified to wait for the next "exposure synch. IN" which is in general not required to be in phase with the excitation cycles. As well, the user can define a sequence of image stack exposures, synchronized to that signal without any USB down communication time delay overhead between exposures within a sequence.

- The exposure run lasts exactly the time in milliseconds that has been specified by the PC application before the exposure start order takes place. It ends when a quartz controlled counter reaches the end of the specified duration time window (exposure duration range: 1ms – 600h).

- Within the exposure run duration, the FPGA is pre-conditioning and sending event coordinate data (simultaneously to running measurements) via USB and signalizes the end of the exposure run via USB and additionally always in real time with a TTL output pulse at "exposure synch. OUT"
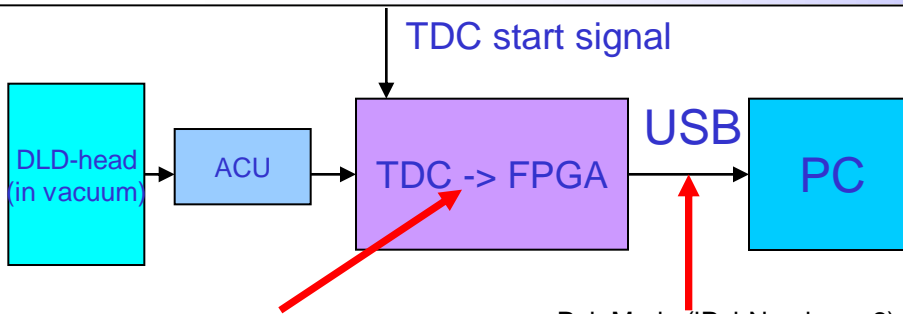
The user must*:
- provide particles to the DLD input at a rate within the specifications: multiple hits of single particles of at least 10 ns time distance, but in average only with a random rate of below 2-8 million hits per second (maximum depends on the individually used DLD type)

The user can, but do not need to*:
- provide an "external TDC start signal IN" for time histogram and/or time resolved image measurements in phase to the source cycle
- provide synchronization signals for exposure run controlling

*** The user must take care about the correct use of the appropriate initialization settings for the used operational mode, respectively.**

SURFACE CONCEPT

TDC start signal

DLD-head (in vacuum) → ACU → TDC -> FPGA → USB → PC

iPairNumber: setup parameter in the DLD_GPX3.INI file section [control] for choosing the general USB transfer mode for TDC data

Data_Format: setup parameter in the DLD_GPX3.INI file section [TDC] for setting of the bit dynamics distribution of x, y, t data for the use of "iPairNumber = 2"

The TDC time results for each event have internally a high dynamics range, i.e. for the used TDC models:

USB2.0-TDC: 19 bits: 2^{19}* 20.576ps ~ 10.7µs

Quad Channel USB2.0-TDC:
23 bits of 6.8587 ps: ~ 40 µs

The FPGA system can use two general data transfer modes in order to stream measured event data via USB:

1. Raw data mode ("iPairNumber = 0"): all TDC data are transferred with full bit dynamics on cost of the maximum transferable event rate (max. rate transferable: 1.8 Mcps)

2. Pair data mode ("iPairNumber = 2"): all 3 event coordinates (x, y, t) are transferred in a 32bit double word, x, y, t bit dynamics ranges are used accordingly the "Data_Format" setting. (max. rate transferable: 7.2 Mcps)

Pair Mode (iPairNumber = 2):
For efficient use of the USB transfer bandwidth, the FPGA transfers the x, y, t coordinates of each event by using a reduced bit dynamics. This is controlled by the set-up switch "Data_Format" (setting can be found in the DLD_GPX3.INI file) which determines how measured x, y, t data sets are packed into a single 32 bit double word for each event. 4 different data formats are possible:

Data_Format = 0:
x: 9bits, y: 9bits, t: 14 bits (image range must fit into 512x512 pixels after ROI and/or binning)
Data_Format = 1:
x: 10bits, y: 10bits, t: 12 bits (image range must fit into 1024x1024 pixels after ROI and/or binning)
Data_Format = 2:
x: 11bits, y: 11bits, t: 10 bits (image range must fit into 2048x2048 pixels after ROI and/or binning)
Data_Format = 3:
x: 12bits, y: 12bits, t: 8 bits (image range must fit into 4048x4048 pixels after ROI and/or binning)

This has consequences for the observable time range, the transferred t-results are representing only the least significant bits of the measured t-results, that is e.g. for data format 0 the least 14 bits. This restriction takes place after time binning is applied to the raw time results. Thus, all measured time results must fit into this restricted bit dynamics window after time binning is applied.

Example for the USB2.0-TDC and data format 0: The *longest observable time distance* between TDC start signal and stop results from the detector can be:
Time binning 1: 2^{14}* (20.576 ps * 1) = *337 ns*
Time binning 2: 2^{14}* (20.576 ps * 2) = *674 ns*
Time binning 4: 2^{14}* (20.576 ps * 4) = *1348 ns (and so on)*

*note: Data_Format does not restrict the resolution, it also does not restrict the dynamics in general, but it limits the observable window (ROI) within the entire dynamics range.
Data_Format is ignored when the system runs in raw data transfer mode ("iPairnumber = 0")

Before you start:

1. Follow the appropriate manual sections for to how to mount the device, about how the cabling must be done, about the correct vacuum pressure ranges, about high voltage drive up procedures, and about the general use and installation of the software.

2. A delay line detector (DLD) is a complicated device, that may respond unexpectedly when one of the many conditions for its correct operation fails. In many aspects it reacts not like other imaging detector systems you may be familiar with. It helps avoiding irreversible damages by mistake or experiencing un-necessary time losses while searching for problems when you follow the "Don'ts" carefully and try to anticipate possible states of violation of the "Don'ts" in your experiment's operation.

3. Avoid operating powerful radio frequency (RF) sources in the vicinity of delay line detector systems. The detector head itself is an efficient RF receiver antenna, that is part of its functionality. Fast switching generators, circuits, and cables around the DLD must be appropriately shielded, any open circuit on such devices may act as RF emitter, disturbing the correct DLD operation. It might be needed to operate the DLD HV inputs through an appropriate RF filter in order to block RF noise from getting this path into the DLD system.

4. Many commercial high voltage (HV) power supplies are generating a lot of RF noise, which can disturb the DLD operation when such supplies are in use for the primary DLD voltages. A simple RC filter in each HV connector line of the DLD helps to avoid or at least reduce disturbances of the DLD operation.

5. Prepare your experiment to have any control element for changing the particle rate load on the detector smoothly from the zero intensity up into a range that can be well operated by the DLD. Such an element could be an adjustable attenuator or an iris aperture in the exciting light beam to give an example. The reason is that the detector has not any possibility to operate in a kind of overload even not by reducing the supplying high voltage on the detector, a very narrow HV window is needed to operate the detector!

Don'ts:

1. Never work with any unknown rate of particle hits going onto the detector, remember, the device is a single counting device, and it responds completely unreliable when you operate it over the limit! In case of any doubt, start without any source and drive up intensity slowly from zero to the wanted operational range.

2. Never operate the detector further, when you observe an unexpected rise of vacuum pressure when applying high voltage (the pressure rises always with the detector load, but it needs some experience to distinguish between normal and dangerous behavior).

3. Never compensate too high count-rates by driving the detector voltage down! Delay line detectors need the high voltage within a very narrow operational window range; driving HV down screws up the correct detector operation completely. Always reduce the incoming particle rate from the experiment to go into the needed operation range!

4. Do never over-expose detector local area parts for a time longer than a second. Overexposed areas are appearing locally dark in the image, while they get so much intensity that the delay line read-out can not see complete sets of events from that regions anymore, so the response is zero rate on such positions! Overexposing ages the micro-channel plates locally, such an aging can later not be compensated by electronics, only by an expensive replacement of the damaged MCP stack.

5. Never expose the detector on limited areas only within the first some hundred hours of operation (burn-in phase). All MCP pores degrade in amplification linearly with the particle loads within the burn-in phase. The time averaged load on all available pores must be nearly homogeneous within the burn-in phase to avoid non-uniform amplifications in different detector areas. If once happened, the only solution is an expensive MCP replacement as well.

6. Never operate the detector while the MCP temperature may be above room temperature.

Checking the correct detector operation before taking the first images:
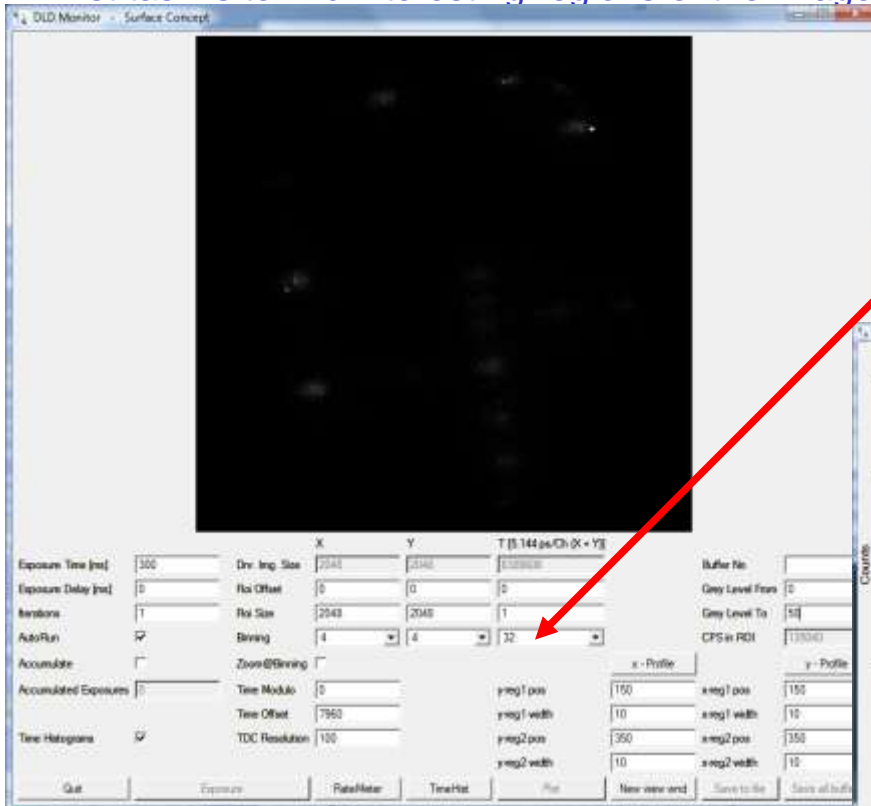
1. Check that all mounting and cabling is made correctly and that the vacuum conditions are in range.

2. First tests should be always done in 2D-imaging mode, i.e without an external TDC start signal. Thus, do not connect your external TDC start signal in the beginning and take care, that the system runs with its internal start, which is set by the parameter "Ext_Gpx_Start = 0" in the DLD_GPX3.INI file.

3. Switch off or attenuate down all particle sources in your experimental setup, so that the expected rate on the detector area is at zero or near by zero.

4. Start the DLDGUI program and press the "Expose" button. The software will run now in live exposure mode. Set the value "Grey level to" from 5 to 1 for the first test (the 3rd parameter on the right of the DLDGUI window), that ensures to observe single hits in the display by eye later on.

5. Drive the detector high voltage slowly up following the manuals recommended timing scheme for the first HV operation at the detector. The procedure can be accelerated when it was already carried out without problems before and no important system status has been changed in between (slow procedure is recommended for the first time after bake-out or venting).

6. Single event hits will appear in the image display of the DLDGUI program when one approaches the correct detector operational voltage (see specification sheet for the correct individual voltage of your detector).

7. Before increasing intensity of the source, it is recommended to accumulate an image from the single hits (dark counts) in order to see whether they are homogeneous distributed over the active detector area.

8. If that works correctly, your detector is ready to use, you may increase the intensity slowly while checking the CPS window to stay in the operating range that is valid for your DLD, observe all changes in live mode.

A few preparations before measuring time resolved:

1. Take care that you can provide a TTL signal as external TDC start signal, which is in phase with the cycle of your excitation source. Its time period must be larger than 140 ns! If your source runs with any smaller period duration, a frequency divider must be used to fulfill that specification. The TDC start signal must be of very good quality in order to measure with sufficiently good time resolution. Be sure that this signal can be loaded by 50 Ohms and reaches with such a load at least 2.1 Volts for the its "high" state. For most DLD systems, the rising edge is used for relative time measurements; its quality may strongly limit the achievable time resolution of your system. The faster the rise time and the smaller the jitter on that edge, the less limitations will take place on the time resolution.

2. Caution: The TDC start input can be damaged, when the input voltage exceeds 5 volts. As well, it is more save for getting stable working conditions when connecting this input while the TDC device is switched off.

3. The DLD hardware can not work correctly with an external TDC start signal acting in parallel with the internal TDC start, which is used for 2D-imaging. Therefore, the "Ext_Gpx_Start" parameter in the DLD_GPX3.INI file must be switched to 1, when working with the external TDC start signal connected on. Caution: When this switch is 1 and the device does not recognize the provided external TDC start signal for any reason, the entire detector system will responds with 0 count rate recognized, independently how many events are going onto the detector area!

4. Prepare yourself to think cyclic, the detector collects time resolved histograms over thousands or millions of cycles of your excitation source. It may be, that some results at the beginning of an observed time histogram cycle length must be considered to be correctly at the end of the considered cycle window!

5. For your convenience, be sure that the external TDC start signal comes in each excitation cycle earlier into the TDC than the stop results from the belonging measured events. This requires to understand, how and when in your source cycle your external TDC start signal is generated and how long the excited particles need to get onto the detector.
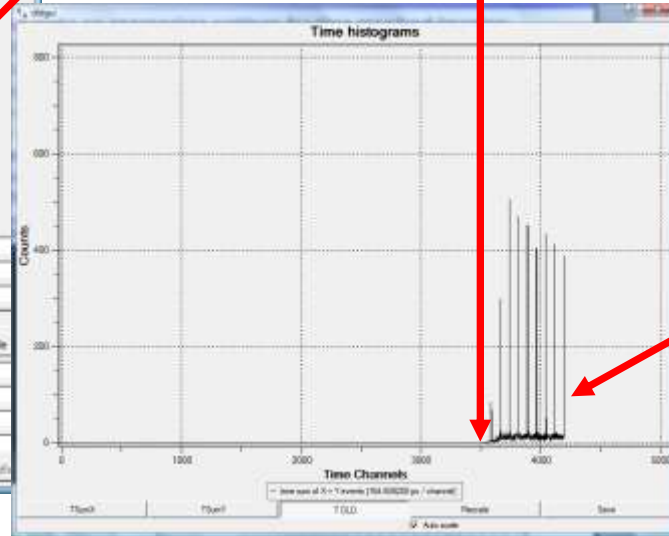
SURFACE CONCEPT

Understand your experiments timing and make appropriate settings for time resolved imaging:

1. Before time resolved imaging can be done, you must check, understand, and (when needed) adjust your time measurement setup. That is because of two reasons: a) the time measurement range of the DLD system is huge but the positions of the interesting time spectra in it can not easily be predicted, because it depends on your experimental setup, b) time resolved imaging relies on memory size definitions and is thus limited by available histogram memory at the computer.

2. One always starts with a time-ROI-offset = 0 and time-ROI-size = 1, that defines to collect a time integrated 2D image only, but you can observe the image integrated time histogram in order to see experimentally, where your interesting time spectrum features are located on the cycle time axis.

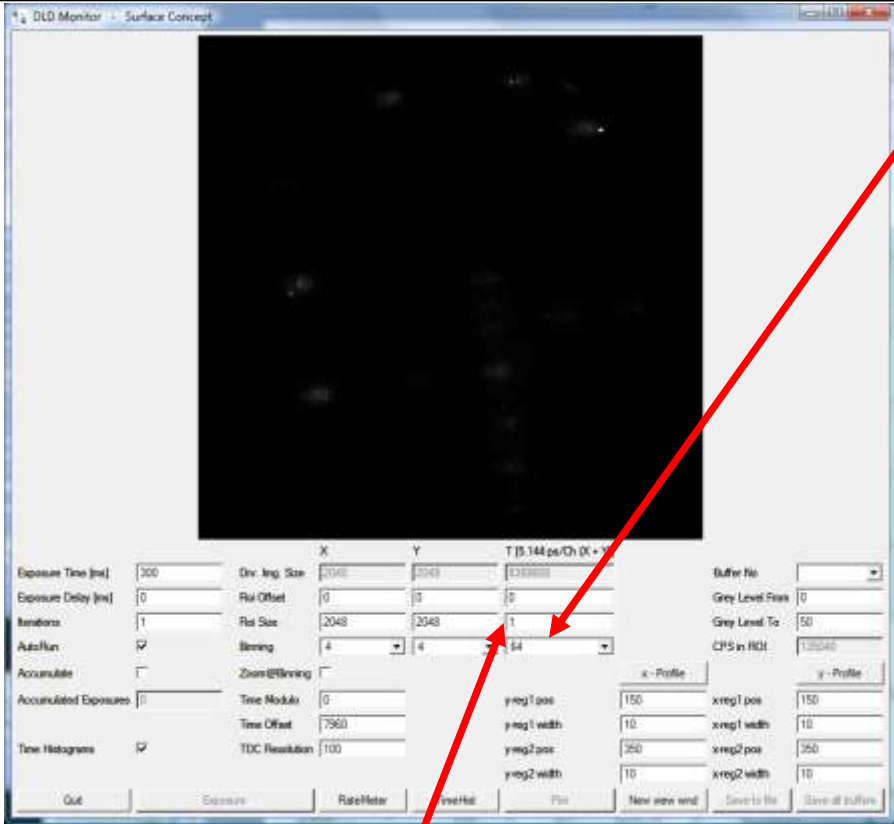3. First task is to find interesting regions of the image integrated 1D time spectrum:

Finding your timing features in the 1D spectrum:
- The length of the time histogram is limited by the Data_Format as described above and the display is limited by the parameter "1D_histo_size" in the DLD_GPX3.INI file in addition
- The time features always have an at least technically unavoidable zero-point offset. Thus, it may be that you see not results in that window at all!
- If so, start to increase the time binning until you get results in your 1D time histogram starting at the channel (offset/time_binning).
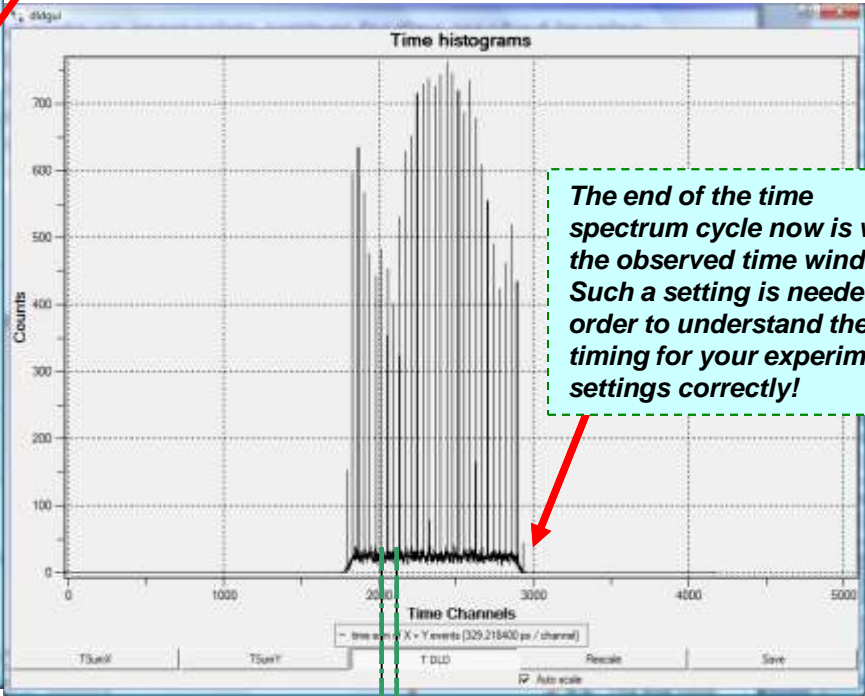
The time features may be first non-visible or appear incomplete or cyclically wrapped, so play with the time binning until you see unambiguous results here!

E.g.: This side could be incomplete depending on your hard- and software settings, larger time binnings will help to show the full distributions!

SURFACE CONCEPT

Finding your timing features in the 1D spectrum:
- In this example, the time-binning was needed to be at least 64 in order to get the complete time spectrum into the 1d time histogram window:

The end of the time spectrum cycle now is within the observed time window! Such a setting is needed in order to understand the timing for your experiments settings correctly!

Important notes:
- Up to here, there is no time resolved imaging used, that is because the time region of interest (ROI(t)) is sill set to ROI(t)-offset = 0 and ROI(t)-size = 1
- In order to collect 3D image stacks, the ROI(t) must be set appropriately.
- Note, that the ROI settings must be made with channel numbers before the binning operation is taking place! That means, when reading ROI values from a 1D time histogram, which can only be displayed with a time binning > 1, the read channel limits must be multiplied with the use time binning number in order to find the appropriate ROI(t) settings for the time resolved imaging.

Example for setting a ROI(t) for time sliced imaging:
- For illustration, we assume to be interested in time sliced imaging the green marked interval from channel 2000 to channel 2100.
- Remember that this 1D display runs with time binning 64, thus the ROI settings must be:
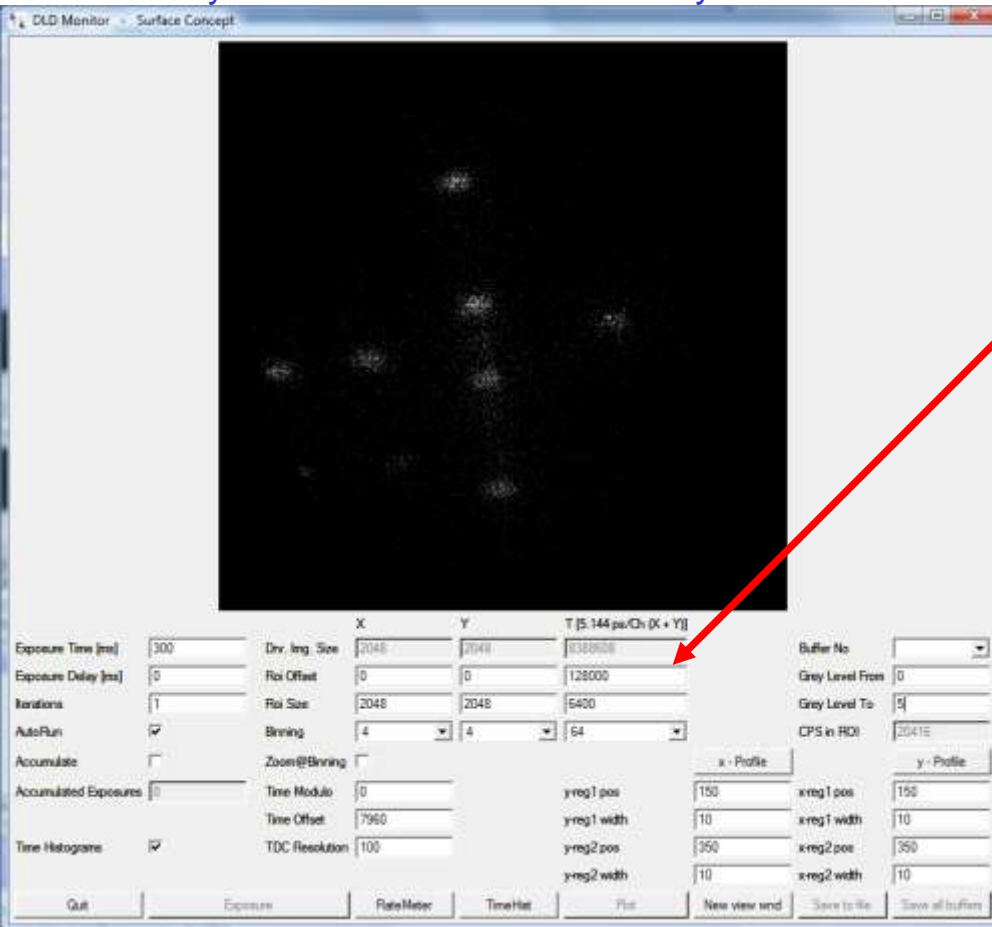
ROI(t)-offset = 2000*64 = 128000
ROI(t)-size = (2100-2000)*64 = 6400
This must be placed into the ROI(t) windows of the DLDGUI:

Acquire time resolved imaging data:

1. Define the ROI in time which you like to acquire in time sliced mode, calculate like explained above.
2. Always stop the live imaging (AutRun off) for making any ROI changes.
3. Take care about the binnings in x, y, and t; be aware that the allocated memory might exceed the available size on your PC. The setting in that example will allocate memory for 100 images (time slices) which corresponds to 6400 time channels in ROI(t) binned by 64. With a time binning of 4, the number of image memory to allocate would increase by a factor of 16 to 1600 images!
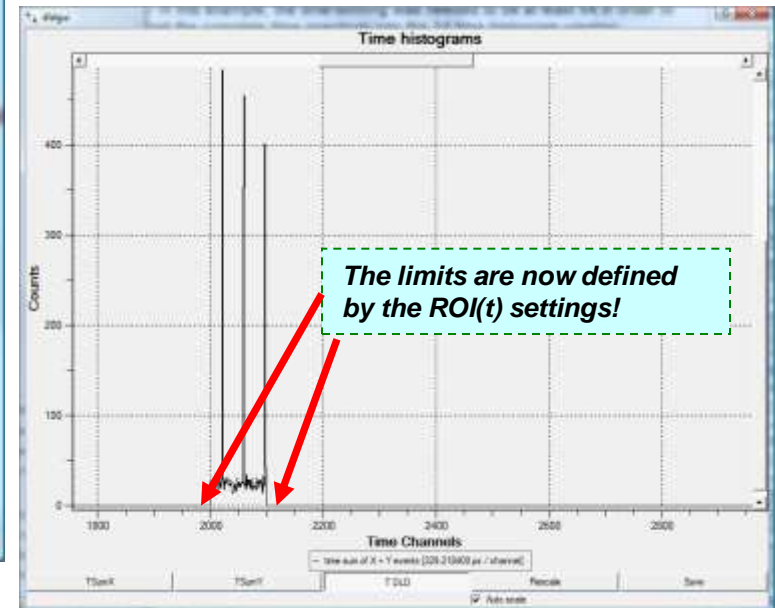

Note:
Time sliced imaging can easily need huge amounts of memory. Use ROI in all 3 coordinates as well as binnings in x, y, and t in order to find the best compromise for the available memory.

Example for setting a ROI(t) for time sliced imaging:

ROI(t)-offset = 2000*64 = 128000
ROI(t)-size = (2100-2000)*64 = 6400
This must be placed into the ROI(t) windows of the DLDGUI:

The limits are now defined by the ROI(t) settings!

SURFACE CONCEPT

Notes about cyclic behavior of time histograms:

1. Depending on your external setup and on the settings of the DLD system, time results from the detector may appear completely within a real or a virtual defined cycle, that has a time zero position in phase with the external TDC start signal.

2. It appears that time result distributions could reach the end of such a cycle interval and be wrapped to the beginning of the cycle window. The situation is illustrated by the both time histogram windows below. In the left panel the distribution is wrapped from channel 2420 back to the cycle beginning (channel 2420 marks the cycle length in that example). In the right panel this inconvenient result could be corrected by placing a delay into the external TDC start signal in order to shorten the time distances between start and stops an so move the distribution far enough to the left being completely in the observed time window.